



HIGHNESSTM

One of a kind

HM483FH111QY

48.3" Stretch Color TFT-LCD

Release Date
21st Nov 2025

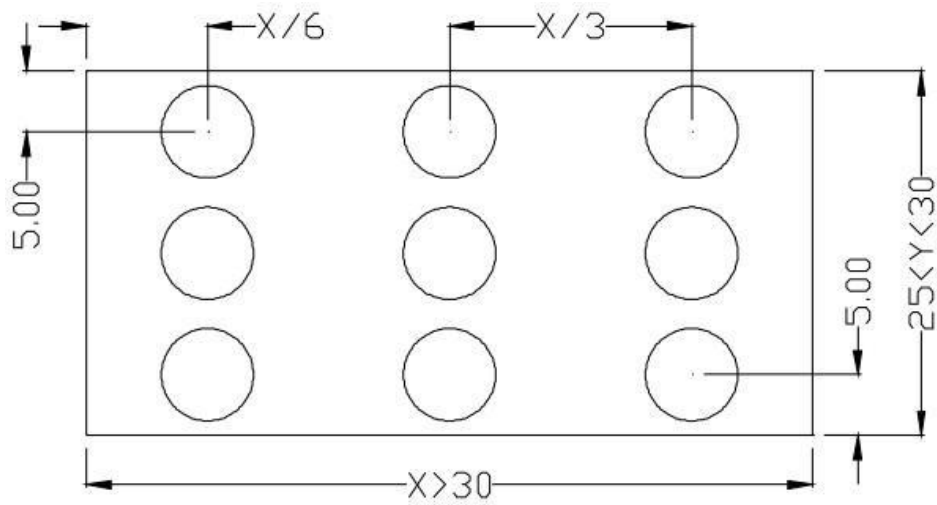
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HIGHNESS MICROELECTRONICS LTD.

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1. General Specification

Item	Specification	Unit
Screen Diagonal	48.3"	inch
Active Area	1209.6(H) x 201.6(V)	mm
Outline Dimension	1240(H) x 232(V)	mm
Resolution	1920(H) x 320(V)	-
Pixel Pitch	0.210 x 0.630	mm
White Luminance	700 (typ)	cd/m ²
Uniformity	≥80	%
Color Temp	≥6500	K
Power Consumption	<49	W
Contrast Ratio	1500	CR
Aspect Ratio	16:2.6	
Viewing Angle	176(H), 176(V)	Deg.
Response Time	14	ms
Mean Expected Lifetime	50,000 h @ 25°C (BLU)	-
Display Color	16.7M	Color
Pixel Arrangement	SRGB >95%	-
Surface Treatment	3H (Haze=1%)	-
LCD Input Voltage	12(type)	Volt
LCD input Current	0.3 (type)	Amper
LCD inrush Current	≤3	Amper
Backlight Type	Edge Light	-
Operating Temp.	-25 ~ +85	°C
Storage Temp.	-35 ~ +85	°C
Humidity	10 ~ 90	%
Weight	< 9.5	Kg



Drawing (2) Uniformity measurement

2. LCD Electrical Specification

2.1 Power Specification

Parameter		Symbol	Value			Unit	Remark
			Min.	Typ.	Max.		
LCD Power Supply Input Voltage		V_{DD}	10.8	12	13.2	[VDC]	
LCD Power Supply Input Current		I_{DD}	-	0.3	0.94	[A]	Note-1
LCD Power Consumption		P_{VDD}	-	10.96	-	[W]	
Inrush Current		I_{RUSH}	-	-	3	[A]	
Frame Rate		Frequency	48	60	62	[Hz]	
CMOS Interface	Input High Threshold	V_{IH}	2.7	-	3.3	[VDC]	
	Input Low Threshold	V_{IL}	0	-	0.6	[VDC]	

Note:

(1). The specified current and power consumption are under the White Pattern, $T_a = 25 \pm 2^\circ \text{C}$.

2.2 LCD Interface description

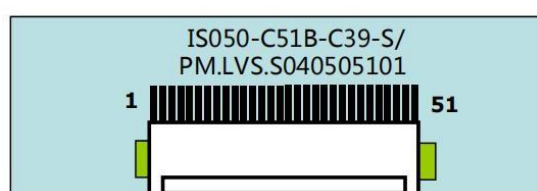
LVDS Connector :IS050-C51B-C39-S or Compatible.

Module connector (CN1) Pin configuration shown on the table below

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I ² C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I ² C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC	Not Connected	48	VCC	Input Voltage +12V
43	NC	Not Connected	49	VCC	Input Voltage +12V

- Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.
2. Input Level of LVDS signal is based on the EIA-644 Standard.

Rear view of LCM



BIST Pattern

PT1:Black (2sec)	PT2:White (2sec)	PT3:Red (2sec)	PT4:Green (2sec)	PT5:Blue (2sec)

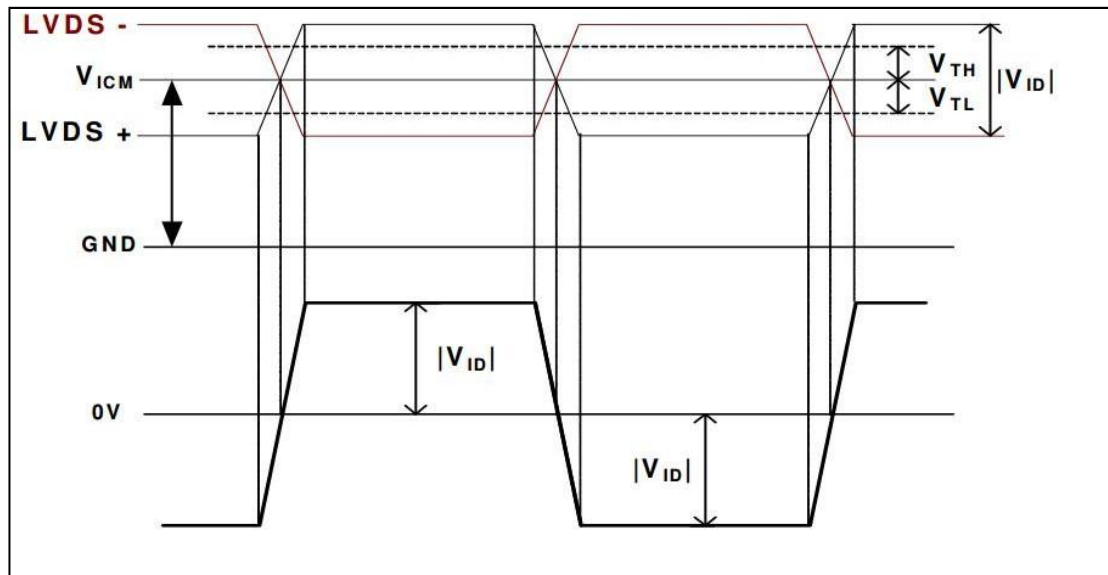
2.3 Signal Electrical Characteristics

2.3.1 DC Characteristics of each signal are as following:

Symbol	Parameter	Min	Type	Max	Units	Condition
V_{TH}	Differential Input High Threshold	-	-	100	[mV]	$V_{CM}=1.2V$
V_{TL}	Differential Input Low Threshold	-100	-	-	[mV]	$V_{CM}=1.2V$
$ V_{ID} $	Input Differential Voltage	100	400	600	[mV]	Note-1
V_{CM}	Differential Input Common Voltage	0.6	1.2	2.4 - $ V_{ID} $ /2	[V]	-

Note:

(1) LVDS Signal Waveform shown as below:

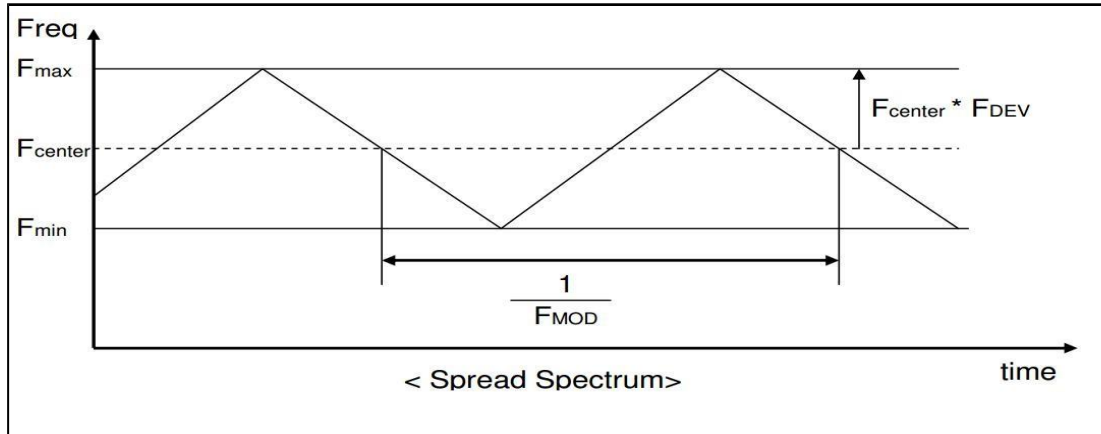


2.3.2 AC Characteristics

Description	Symbol	Min	Max	Unit	Note
Max deviation of input clock Frequency during SSC	F_{DEV}	-	± 3	%	Note-1
Max modulation frequency of input clock during SSC	F_{MOD}	-	200	kHz	Note-1

Note:

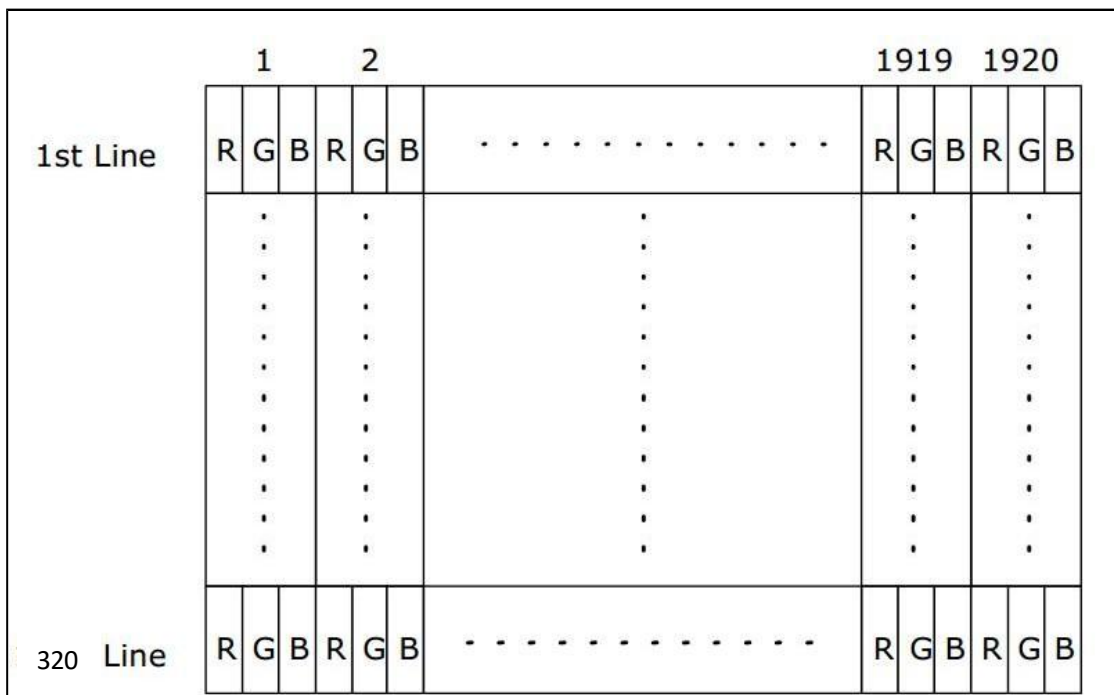
(1). Show as below:



2.4 Signal Characteristics

2.4.1 Pixel Format Definition

Following figure shows the relationship of the input signal and LCD pixel format:



2.5. Timing Characteristics

The input signal timing specifications are shown as the following table:

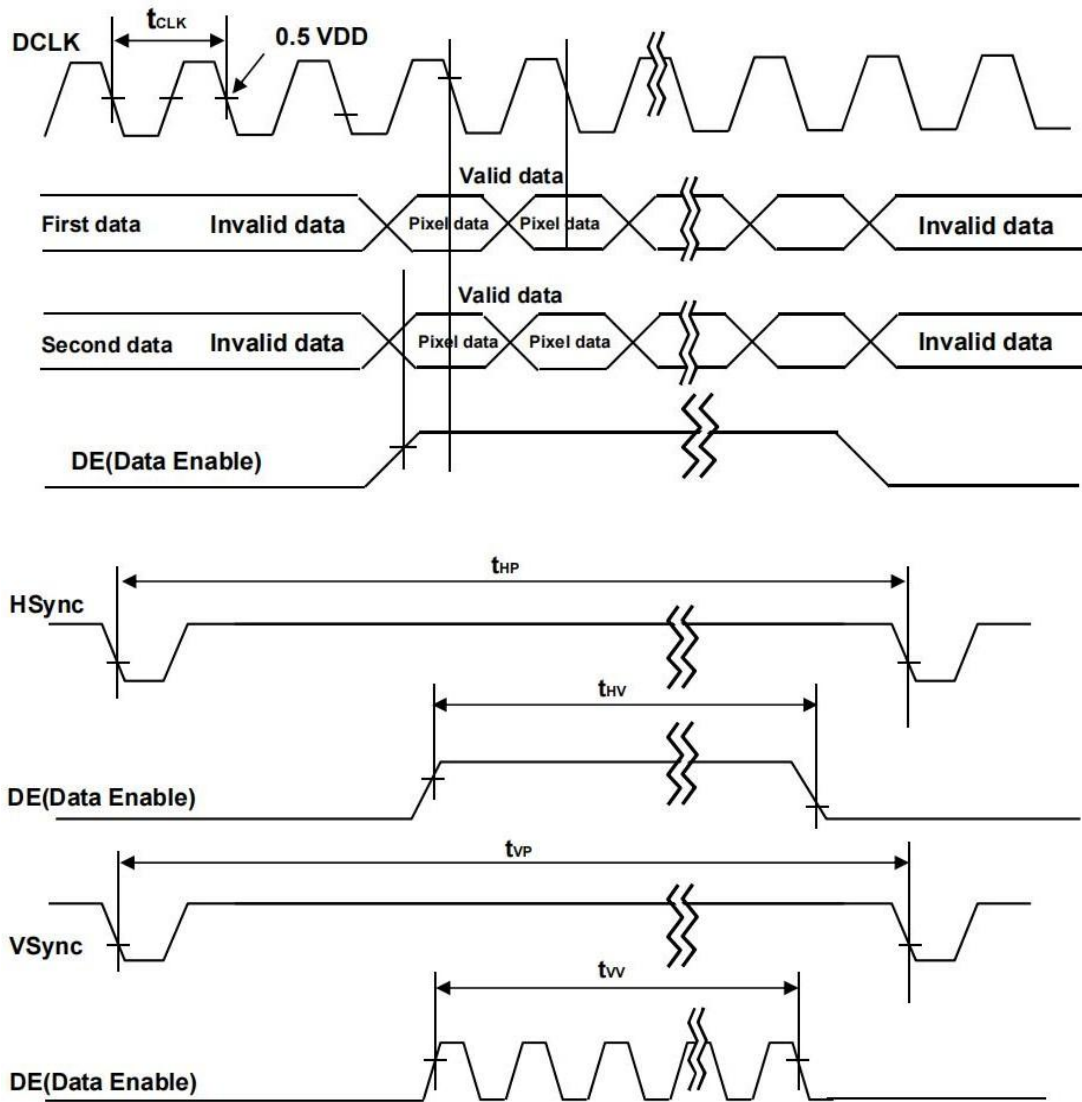
Item		Symbols	Min	Typ	Max	Unit	
Clock	Frequency	1/Tc	60	74.25	78	MHz	
	High Time	Tch	-	4/7Tc	-		
	Low Time	Tcl	-	3/7Tc	-		
Frame Period		Tv	1100	1125	1149	lines	
			48.5	60	63	Hz	
Horizontal Active Display Term		Valid	t _{HV}	-	960	-	t _{CLK}
		Total	t _{HP}	1060	1100	1200	t _{CLK}
Vertical Active Display Term		Valid	t _{VV}	-	1080	-	t _{HP}
		Total	t _{VP}	1100	1125	1149	t _{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

< Table 9. LVDS Input SSCG >

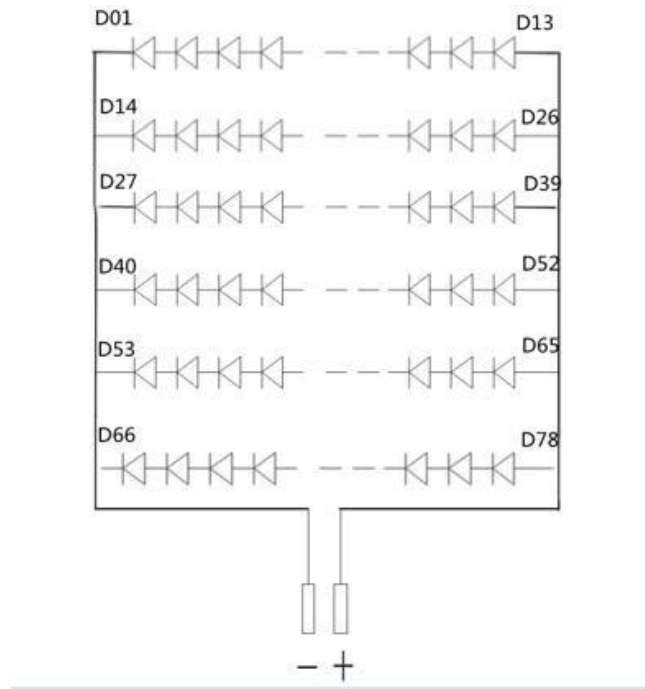
Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	45	74.25	85	MHz
T _{LVSK}	LVDS channel to channel skew	F=100MHz V _{IC} =1.2V V _{ID} =±400mV	-380	-	+380	ps
F _{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F _{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T _{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

2.6 Timing diagram



3. Backlight Specifications

3.1. Light Bar Diagram



Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	IF	—	150	—	mA	One lamp bead
Forward Voltage	VF	2.8	—	3.4	V	One lamp bead
Power consumption	Pd	32.76	—	39.78	W	One Lightbar
Single lamp luminous flux	φ	55	—	—	lm	One lamp bead

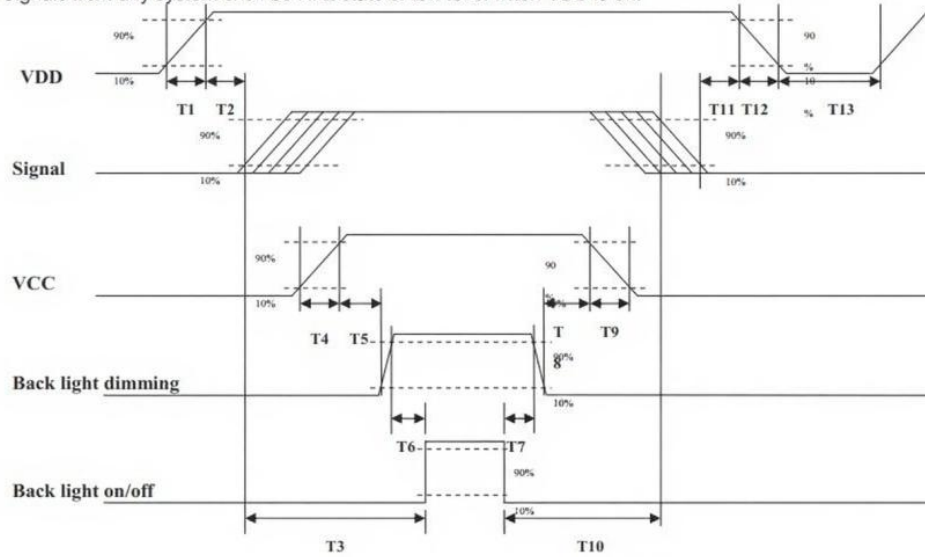
3.2 Light Bar Cable

TBD

Item	Unit	Typ	Remark
Brightness	Cd/m ²	700	
BLU Current	A	0.726	
BLU Voltage	V	36.5	
Power Consumption	W	26.5	
Temperature	°C	35	Lightbar side

3.3 Power on/off sequence for LCD

VDD power and LED on/off sequence are as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power ON/OFF sequence timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	0	40	50	[ms]
T3	200	-	-	[ms]
T4	0.5	-	10	[ms]
T5	10	-	-	[ms]
T6	10	-	-	[ms]
T7	0	-	-	[ms]
T8	10	-	-	[ms]
T9	-	-	10	[ms]
T10	110	-	-	[ms]
T11	0.5	16	50	[ms]
T12	-	-	100	[ms]

4. Reliability Test

Environment test conditions according to **EN50155**

Items	Required Condition	Note
Temperature Humidity Bias	Ta=50 Degree,80%RH,300H	
High Temperature Operation	Ta=50 Degree,60%, 300H	
Low Temperature Operation	Ta=0 Degree,300H	
High Temperature Storage	Ta=70 Degree,60%RH,300H	
Low Temperature Storage	Ta=-25 Degree,300H	
Shock Test(Non-Operating)	50G,20ms,Half-sine wave,(±X, ±Y, ±Z)	
Vibration Test(Non-Operating)	1.5G,(10-200HZ,P-P),30Min/axis(X,Y,Z)	
On/Off test	On-10s,Off-10s,30000cycles	
ESD	Contact Discharge:±6KV,150pF,1s,8 points,25 times/point.	
	Air Discharge:±8KV,150pF.1s, 8 points, 25times/point.	

Mechanical Dimensions

