HM290FH111QY

29" Stretch Color TFT-LCD

Release Data
21st Nov 2025

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1. General Specifications

Item	Specification	Unit
Screen Diagonal	29"	inch
Active Area	698.4(H) x 221.85(V)	mm
Outline Dimension	726.58(H) x 252.84(V)	mm
Resolution	1920(H) x 610(V)	-
Pixel Pitch	0.36375 x 0.36375	mm
White Luminance	700 (typ)	cd/m^2
Uniformity	⩾80	%
Color Temp	⩾6500 ± 500	K
Power Consumption	<40	W
Contrast Ratio	5000:1	CR
Aspect Ratio	16:5	
Viewing Angle	178(H), 178(V)	Deg.
Response Time	9.5	ms
Mean Expected Lifetime	65,000 h @ 25°C (BLU)	-
Display Color	16.7M	Color
LCD Input Voltage	12(type)	Volt
LCD input Current	0.6 (type)	Amper
LCD inrush Current	⩽1.56	Amper
Backlight Type	Edge Light	-
Operating Temp.	0 ~ +50	°C
Storage Temp.	-25 ~ +60	°C
Humidity	10 ~ 90	%

Note:

(1) Active Area Dimensions: Horizontal=HA, Vertical=VA

(2) Uniformity measurement: Min（5points）/Max(5 points) X100%. Measurement setup according to Figure1

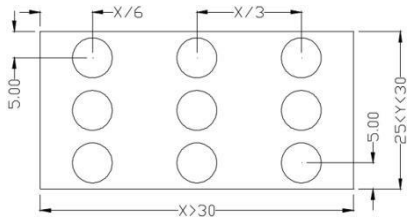


Figure (1) Uniformity measurement

(3) Measurement setup according to the original OC data sheet

(4) Valid for LED backlight unit

2. LCD Electrical Specification

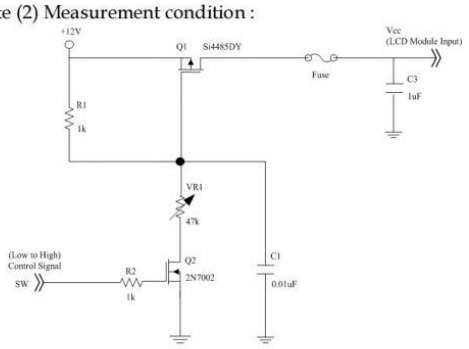
2.1 Power Specification

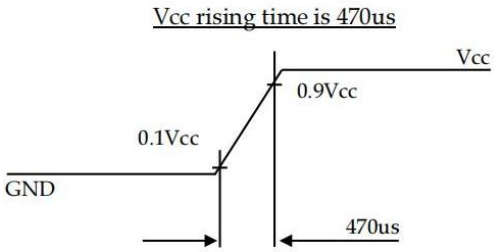
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	–	–	1.56	A	(2)
Power Consumption	White Pattern	P_T	–	7.06	7.76	W	(3)
	Black Pattern	P_T	–	4.30	4.73	W	
	Horizontal Stripe	P_T	–	6.88	7.57	W	
Power Supply Current	White Pattern	–	–	0.60	0.73	A	
	Black Pattern	–	–	0.37	0.45	A	
	Horizontal Stripe	–	–	0.60	0.72	A	

Note (1) The module should be always operated within the above ranges.

The ripple voltage should be controlled under 10% of Vcc (Typ.).

Note (2) Measurement condition :





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

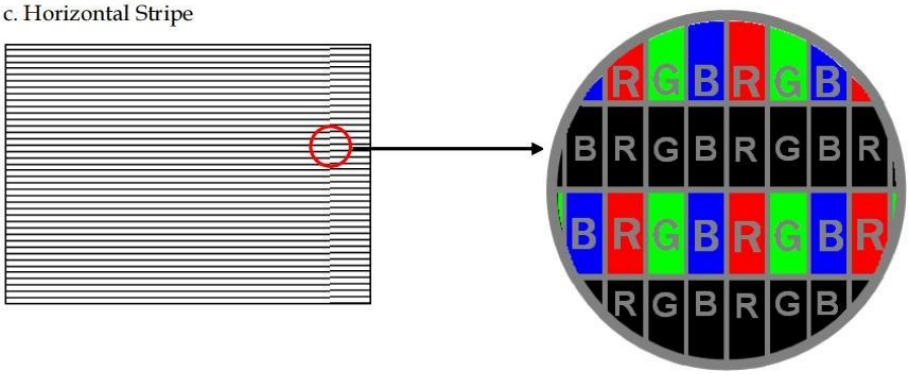
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Horizontal Stripe



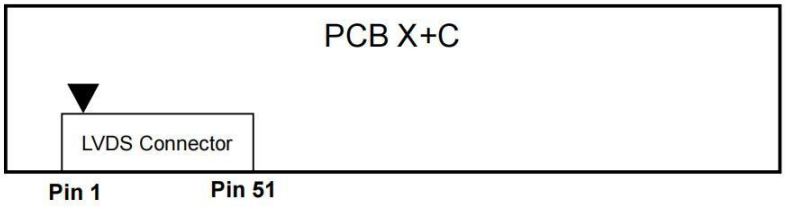
2.2 LCD Interface connections

CNX11 Connector Pin Assignment: [187059-51221 (P-Two), WF23-402-5133(FCN)]

Pin	Name	Description	Note
1	NC	No connection	(2)
2	SCL	I2C clock (For Vcom tunning)	(8)
3	SDA	I2C data (For Vcom tunning)	(8)
4	NC	No connection	(2)
5	NC	No connection	
6	NC	No connection	
7	SELLVDS	LVDS data format Selection	(3)(4)
8	NC	No Connection	(2)
9	NC	No Connection	
10	NC	No connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input.	(5)
20	OCLK+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input	(5)
36	ECLK+	Even pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	

46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin orderdefined as below



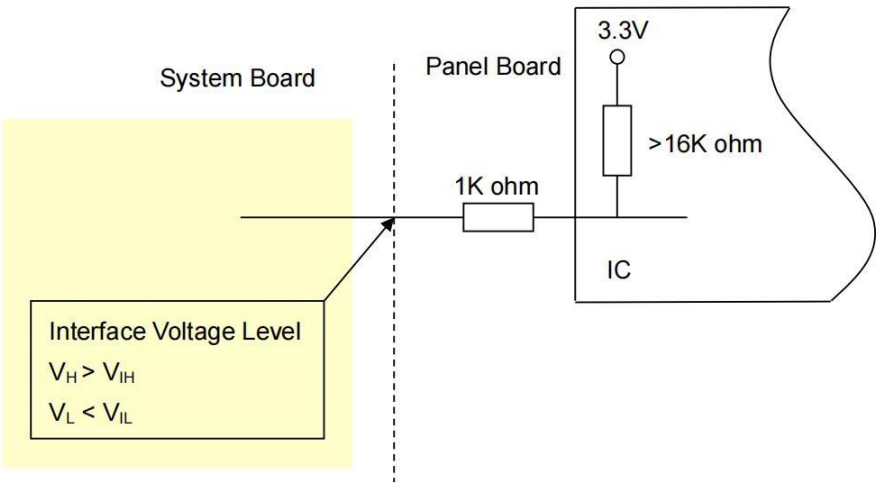
Note (2) Reserved for internal use. Please leave it open.

Note (3) Connect to Open or +3.3V: VESA Format, connect to GND: JEIDA Format.

SELLVDS	Mode
H(default)	VESA
L	JEIDA

L : Connect to GND, H: Connect to +3.3V

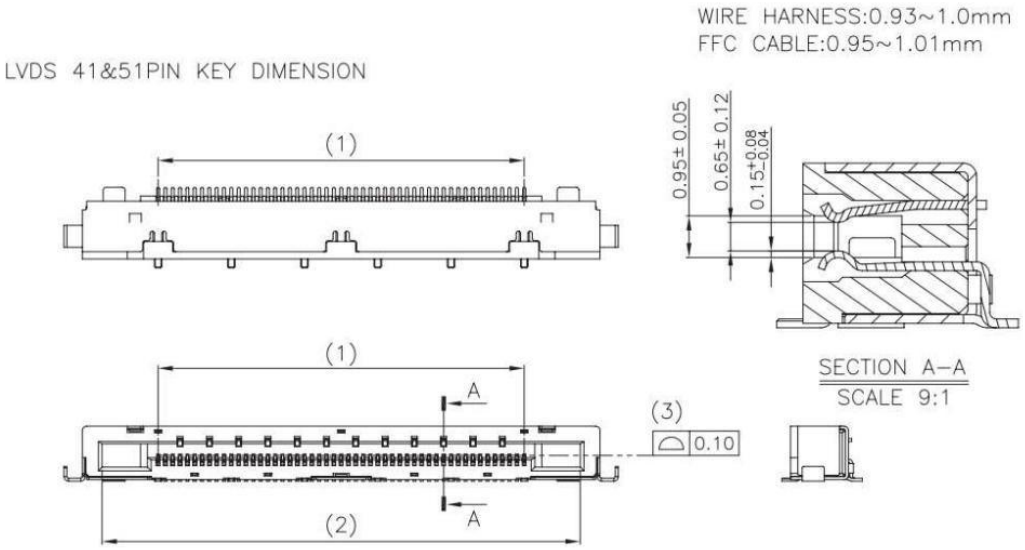
Note (4) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

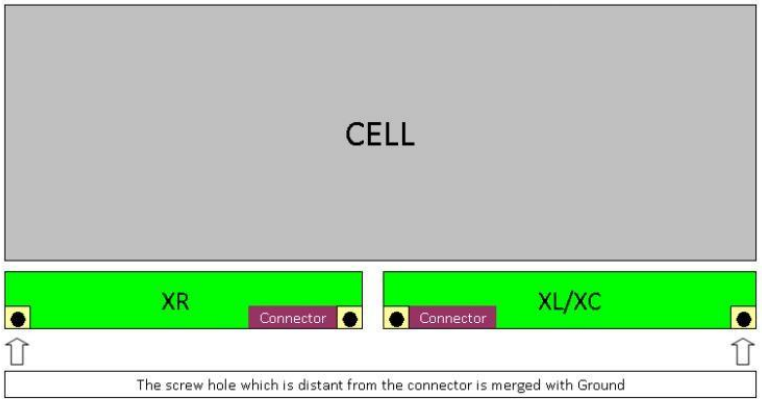
Note (6) LVDS connector mating dimension range request is 0.93mm~1.0mm as below. (Lock type)

LVDS connector Recommend Mating FFC drawing as below (FFC type)

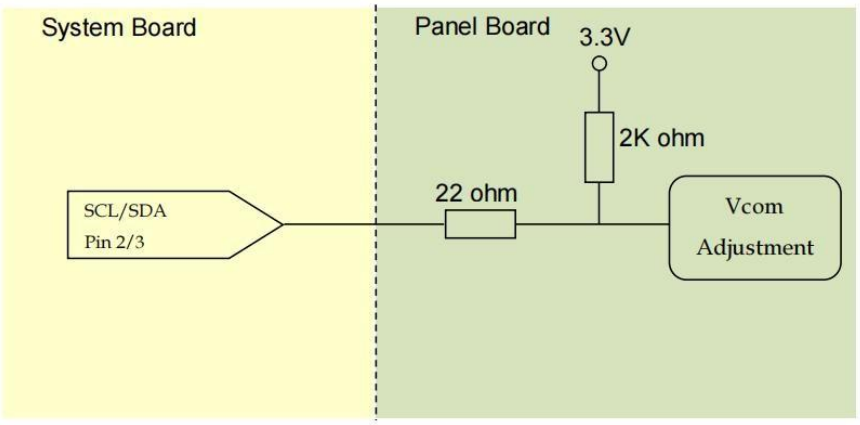


	DIM1	DIM2
41P	20.0± 0.15	27.65± 0.08
51P	25.0± 0.15	32.65± 0.08

Note (7) The screw hole which is distant from the connector is merged with Ground.



Note (8) I2C pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



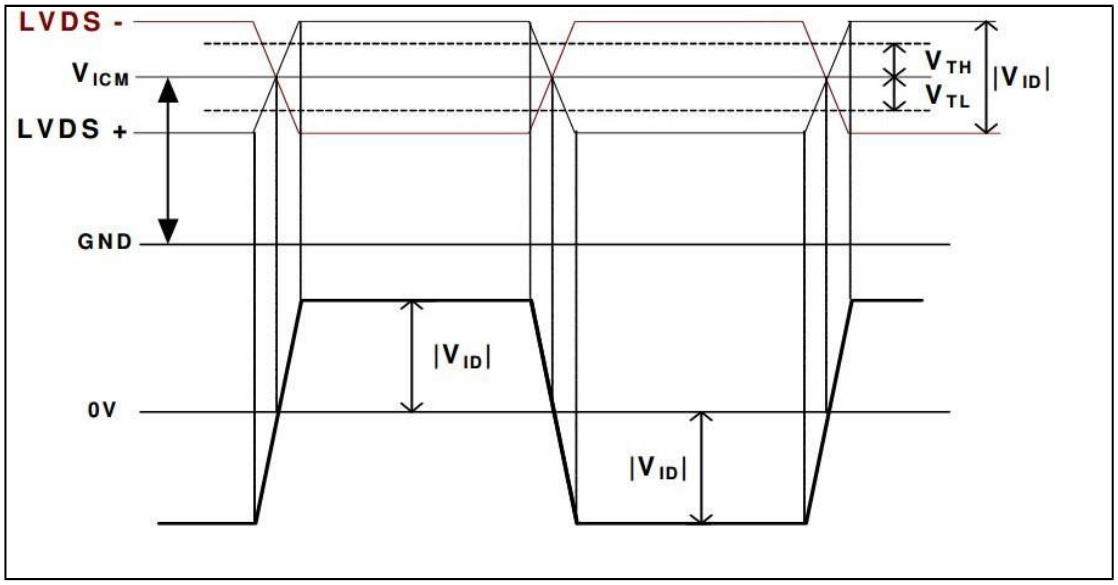
2.3 Signal Electrical Characteristics

2.3.1 DC Characteristics of each signal are as following:

Symbol	Parameter	Min	Type	Max	Units	Condition
V_{TH}	Differential Input High Threshold	-	-	+100	[mV]	V_{CM}=1.2V
V_{TL}	Differential Input Low Threshold	-100	-	-	[mV]	V_{CM}=1.2V
$\|V_{ID}\|$	Input Differential Voltage	100	-	600	[mV]	Note-1
V_{CM}	Differential Input Common Voltage	1	1.2	1.4	[V]	-

Note:

(1) LVDS Signal Waveform shown as below:

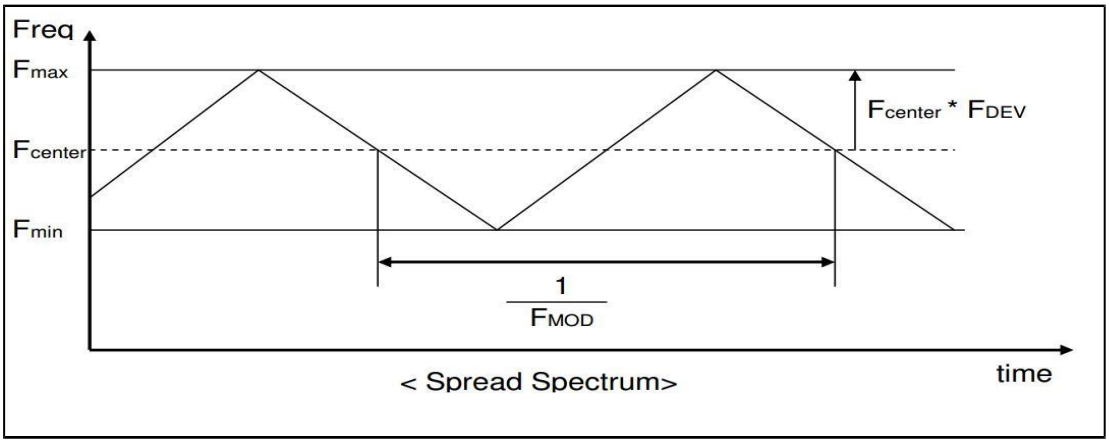


2.3.2 AC Characteristics

Description	Symbol	Min	Max	Unit	Note
Max deviation of input clock Frequency during SSC	F_{DEV}	-	*±3*	%	Note-1
Max modulation frequency of input clock during SSC	F_{MOD}	-	*200*	kHz	Note-1

Note:

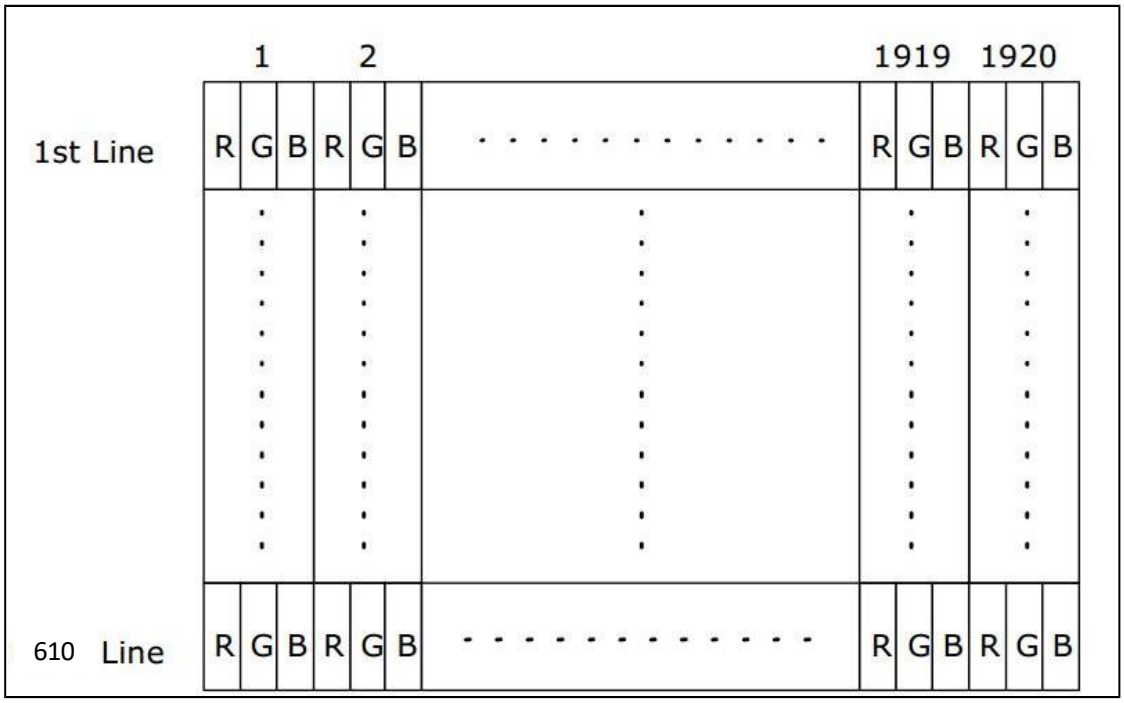
(1).Show as below:



2.4 Signal Characteristics

2.4.1 Pixel Format Definition

Following figure shows the relationship of the input signal and LCD pixel format:

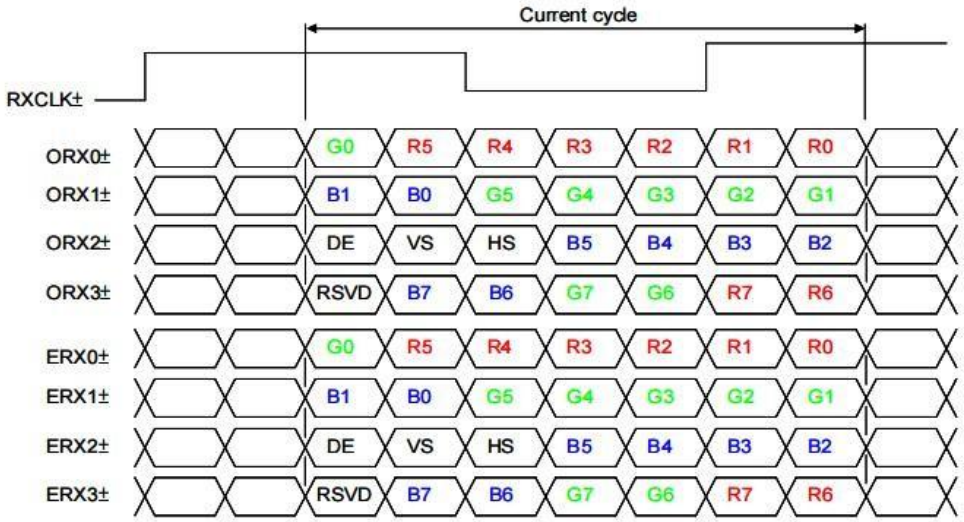


2.4.2 LVDS Data Format

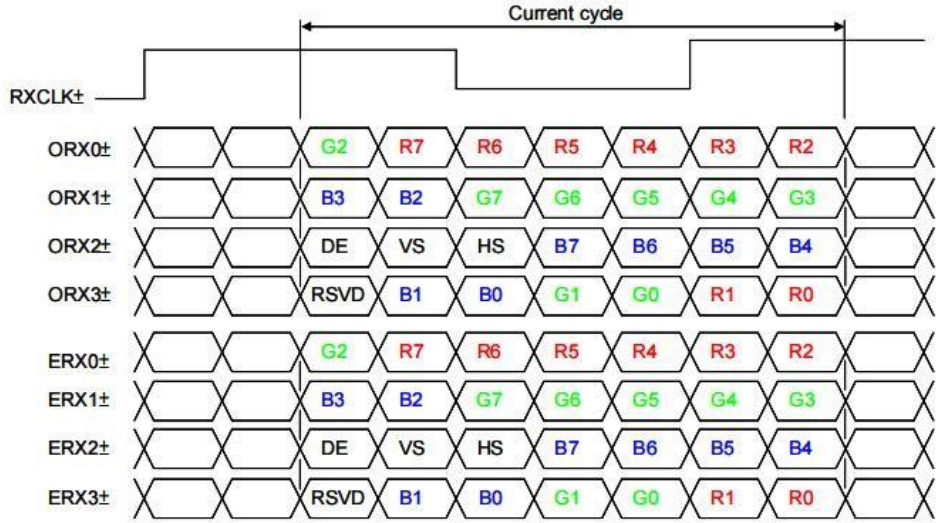
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format



JEDIA LVDS format



R0~R7	Pixel R Data (7; MSB, 0; LSB)	DE	Data enable signal
G0~G7	Pixel G Data (7; MSB, 0; LSB)	DCLK	Data clock signal
B0~B7	Pixel B Data (7; MSB, 0; LSB)		

Note (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

2.4.3 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

2.5. Timing Characteristics

The input signal timing specifications are shown as the following table and timing diagram.

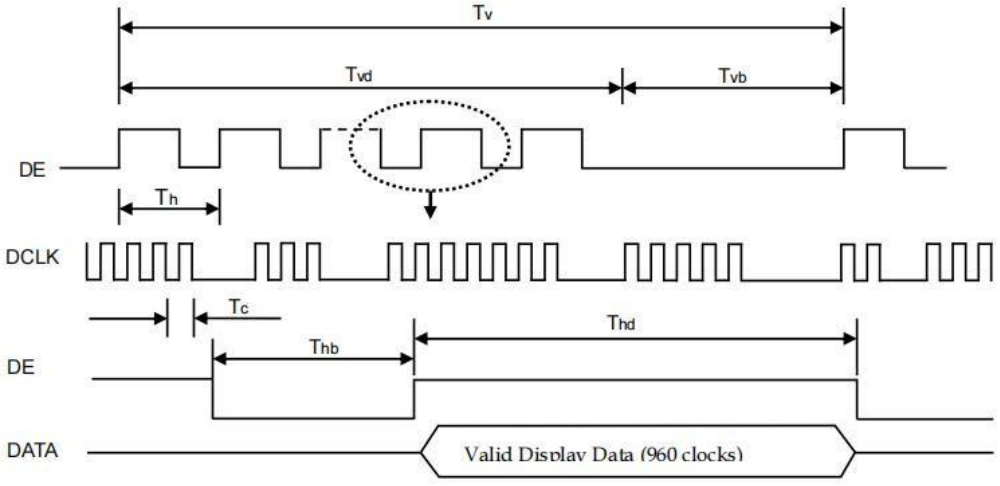
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	–	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	–	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	–	–	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	–	400	ps	(5)
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1100	1125	1480	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	–
	Blank	Tvb	20	45	400	Th	–
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	–
	Blank	Thb	70	140	365	Tc	–

Note (1) Please make sure the range of pixel clock has follow the below equation :

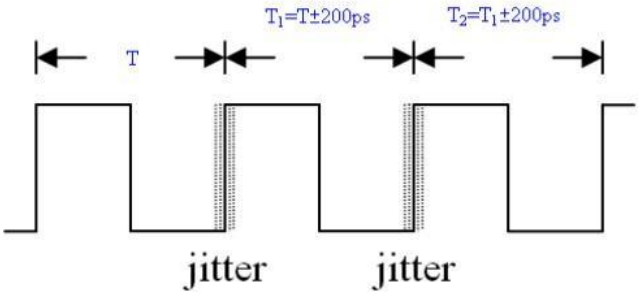
$Fclkin(max) \geqq Fr6 \times Tv \times Th$

$Fr5 \times Tv \times Th \geqq Fclkin\ (min)$

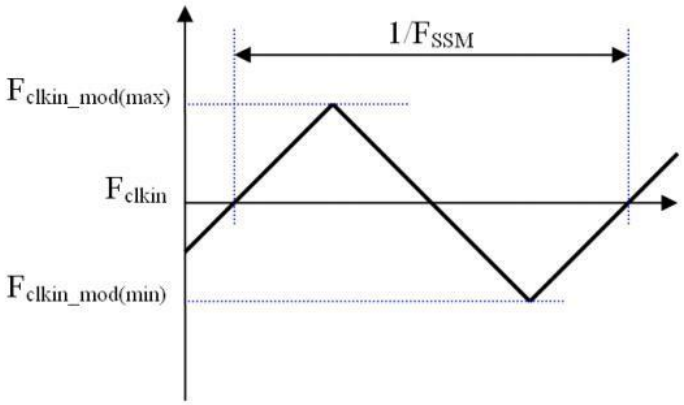
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :



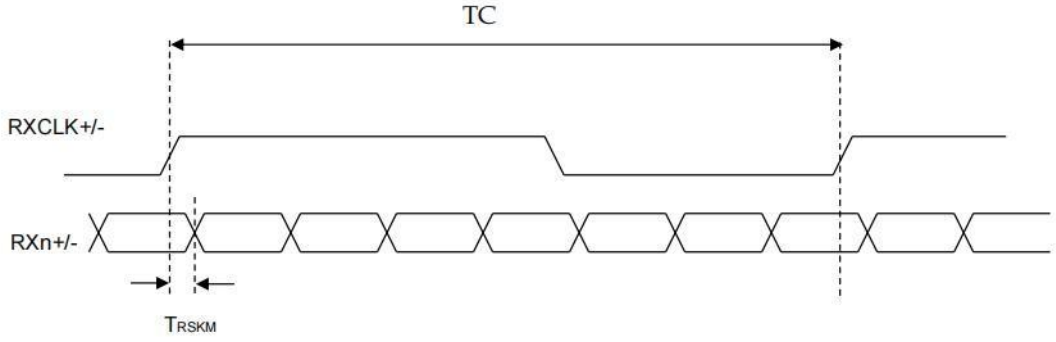
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = | $T_1 - T$ |



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

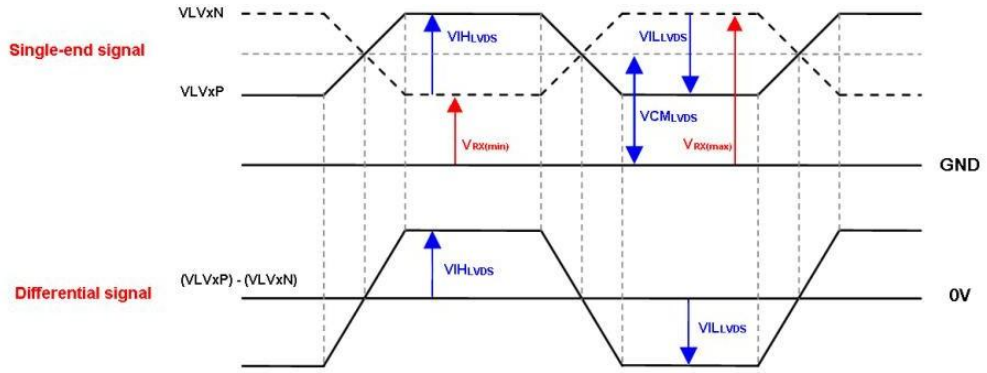


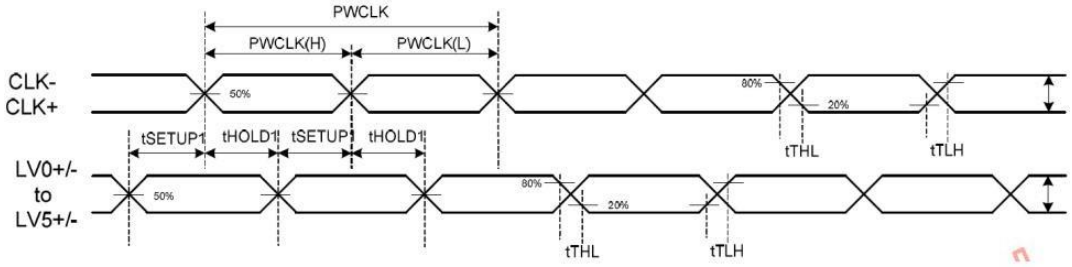
Note (5) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.



2.6 Timing diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
mini-LVDS power Voltage	V_{DD}	2.3	3.3	3.6	V	
mini-LVDS high input voltage	$\|VIH_{LVDS}\|$	175	-	-	mV	Fmax ≦ 340MHz
mini-LVDS low input voltage	$\|VIL_{LVDS}\|$	175	-	-	mV	Fmax ≦ 340MHz
mini-LVDS input voltage range	V_{RX}	0	-	V_{DD}	V	
mini-LVDS common mode input voltage range	VCM_{LVDS}	0.5	1.2	V_{DD}-1.2	V	VCM_{LVDS} = (VCLKP + VCLKN) / 2 or VCM_{LVDS} = (VLVxP + VLVxN) / 2
Data setup time	tSETUP1	0.45	-	-	ns	
Data hold time	tHOLD1	0.45	-	-	ns	
CLK Rising Time	tTLH	-	-	0.7	Ns	From VIL_{LVDS} to VIH_{LVDS}
CLK Falling Time	tTHL	-	-	0.7	ns	From VIH_{LVDS} to VIL_{LVDS}



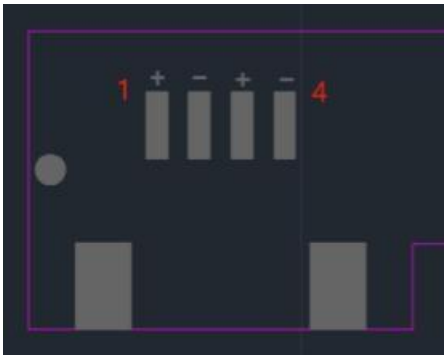


3. Backlight Specifications

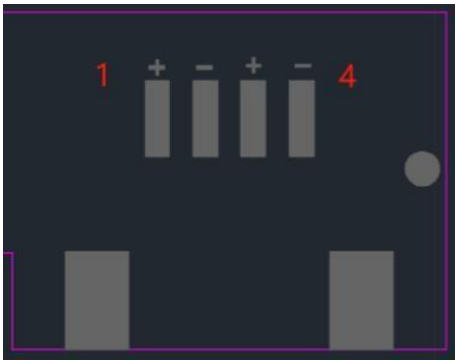
3.1. Backlight led pin define

Connector type:4 x JST SM04B-SRSS-TB

Lightbar Left Side:



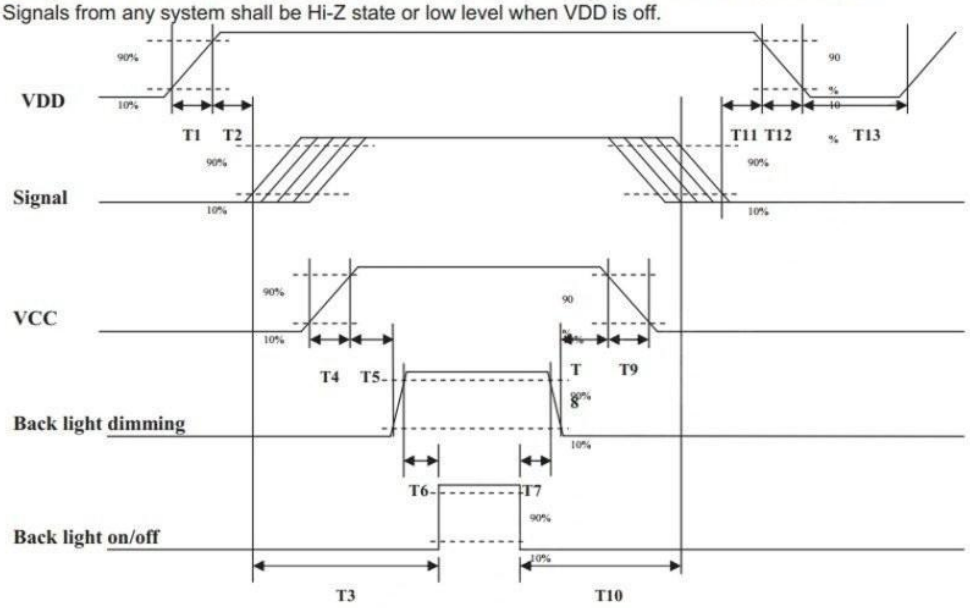
Lightbar Right Side:



Spec.	Unit	Typ	Remark
Luminance	Cd/m^2	700	
BLU current	A	0.455	
BLU voltage	V	38.17	
Power consumption	W	17.61	
Temp.	℃	35	Light bar side

3.3 Power on/off sequence for LCD

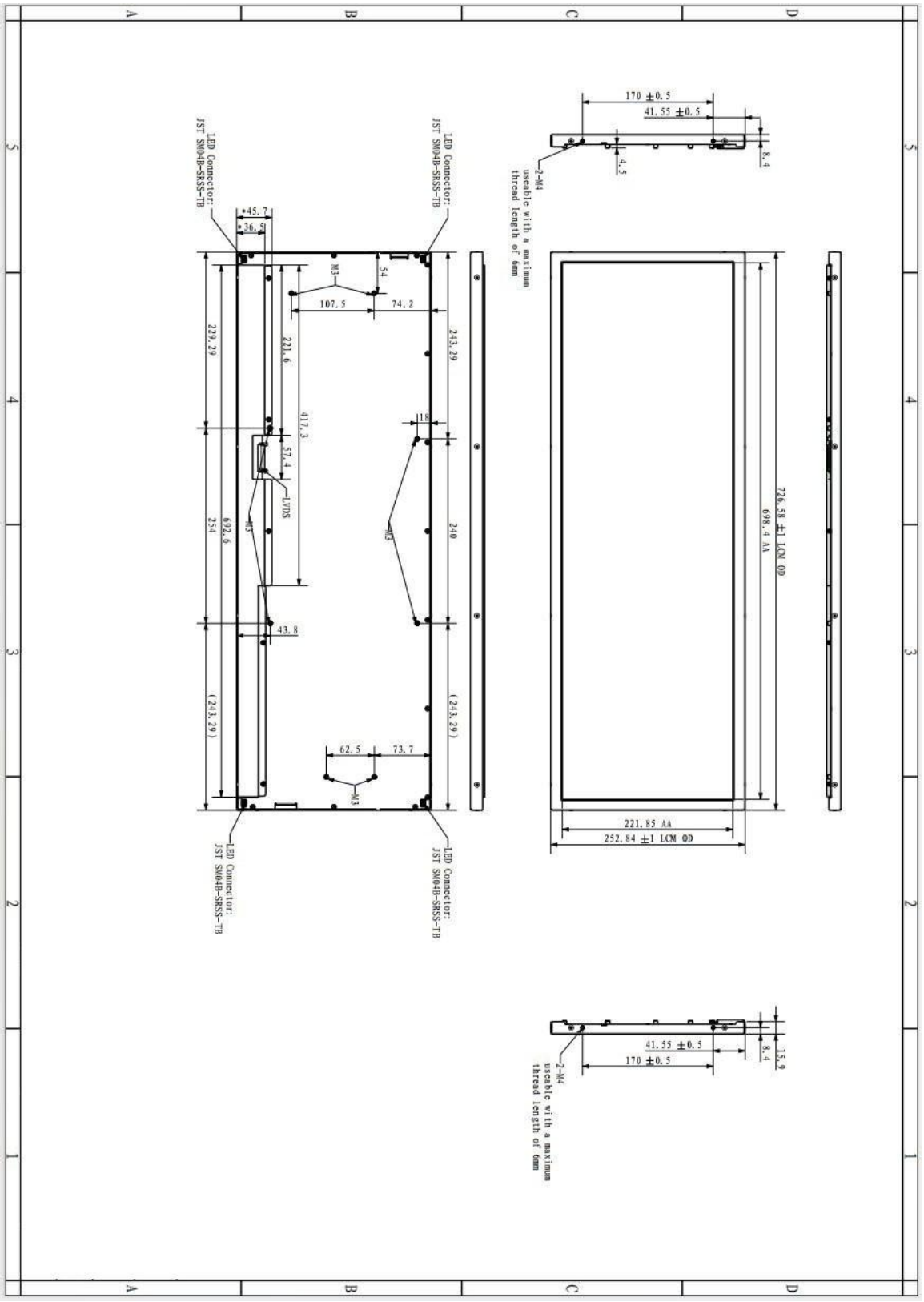
VDD power and LED on/off sequence are as follows. Interface signals are also shown in the chart.
Signals from any system shall be Hi-Z state or low level when VDD is off.



Power ON/OFF sequence timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	0	40	50	[ms]
T3	200	-	-	[ms]
T4	0.5	-	10	[ms]
T5	10	-	-	[ms]
T6	10	-	-	[ms]
T7	0	-	-	[ms]
T8	10	-	-	[ms]
T9	-	-	10	[ms]
T10	110	-	-	[ms]
T11	0.5	16	50	[ms]
T12	-	-	100	[ms]

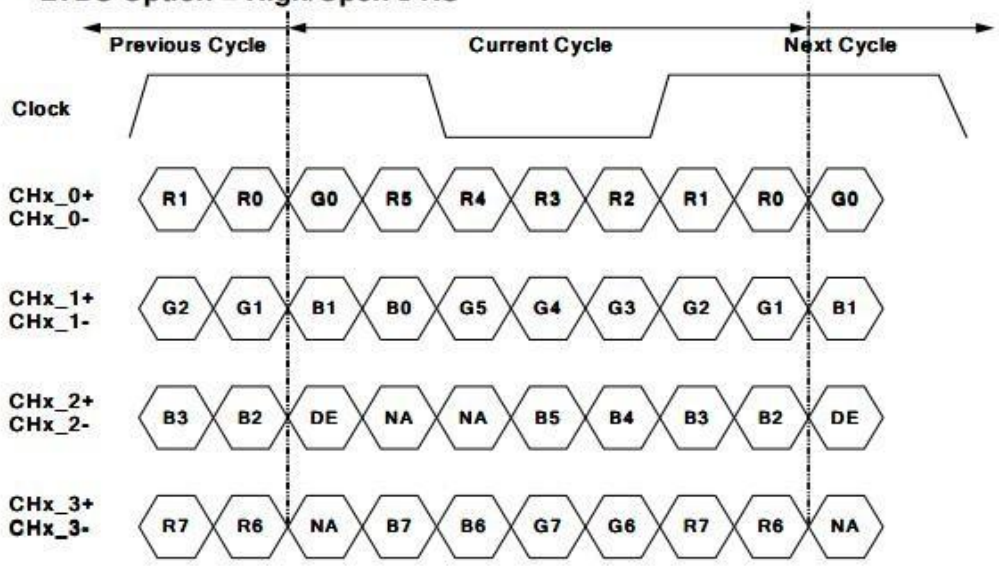
4. Mechanical Dimensions



#APPENDIX-1

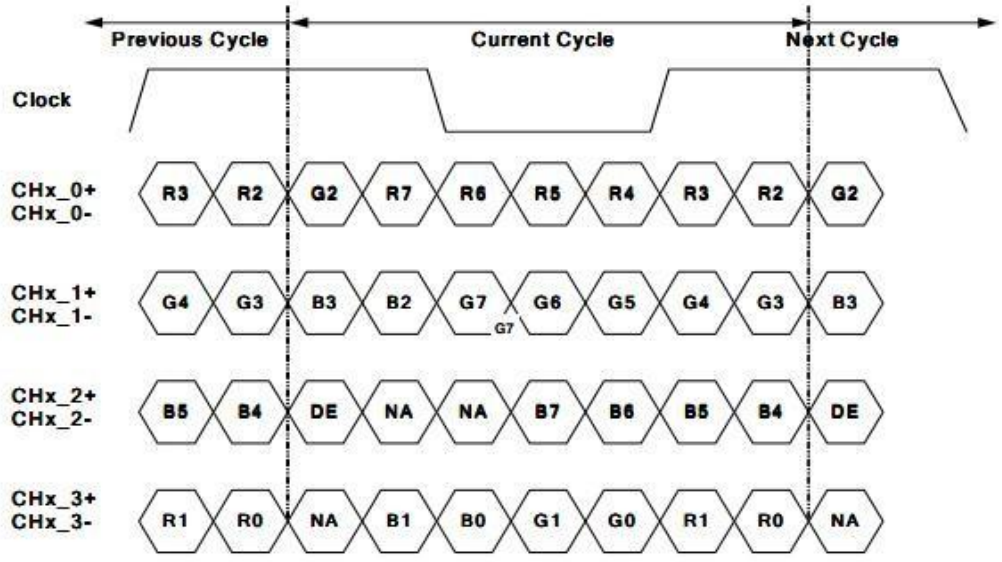
LVDS Select : NS and JEDIA model:

- **LVDS Option = High/Open➔NS**



Note: x = 1, 2, 3, 4…

- **LVDS Option = Low➔JEIDA**



Note: x = 1, 2, 3, 4…