



HIGHNESSTM

One of a kind

HM280FH11B

28" Stretch Color TFT-LCD

Release Date
26th Mar 2021

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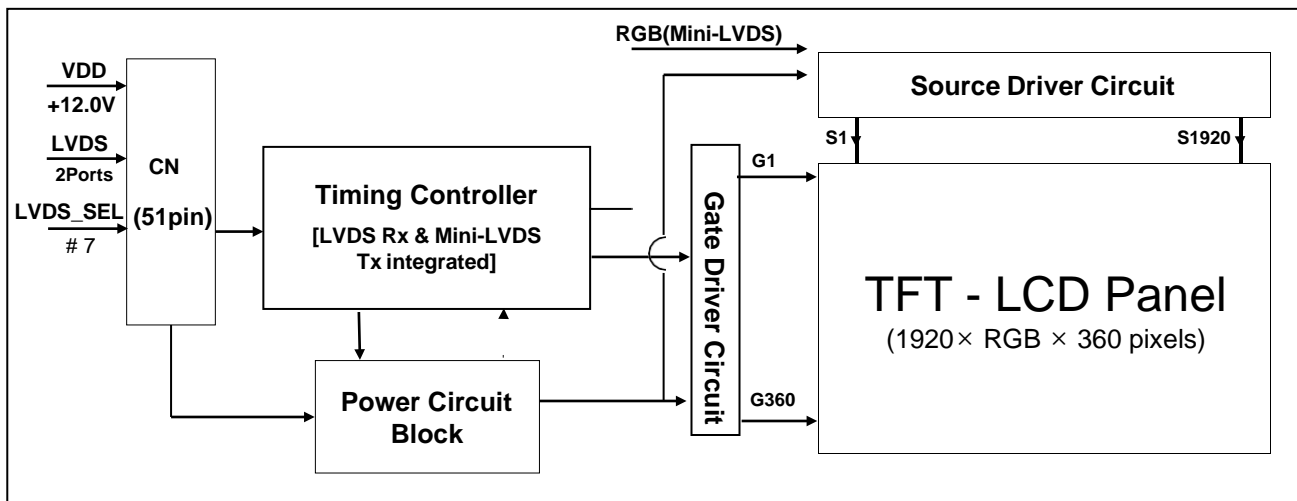
URL: www.highnessmicro.com, Email: sales@highnessmicro.com

1.0 General Description

1.1 Introduction

M280FH111B is a color active matrix TFT LCD Module using amorphous silicon TFT's (Thin Film Transistors) as an active switching device. This Module has a 28inch diagonally measured active area with FHD resolutions (1920 horizontal by 360 vertical pixel array).

Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this Module is adapted for a low reflection and higher color type.



1.2 Features

- Cutting efficiency 90.5%, panel transmittance 6%
- 4 shot normal design, High Response Time 8ms
- Matrix Vcom design (1/3);
- Lightweight design, Body 8.9mm, Depth 16.8mm
- Array process: 1+4mask, AT: 2G3D, Q-CT: 2G3D (S/B detection)
- RoHS compliant

1.3 Application

- TFT-LCD Display for transportation system and financial system
- Display Terminals for diversified information

1.4 General Specification

Parameter	Specification	Unit
Active Area	699.84(H)*131.22(V)	mm
Number of Pixels	1920(H)×360(V)	pixels
Pixel Pitch	121.5×364.5	um
Pixel Arrangement	Pixels RGB stripe arrangement	
Display Colors	16.7M(8bits)	colors
Display Mode	ADS	
Brightness	700	nit
MDL Outline	732(H)x165(V)	mm
MDL Thickness	16.8	mm
Power Consumption	24.8 (Logic: 4.2, BLU: 20.6)	watt

2.0 Absolute Maximum Ratings

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

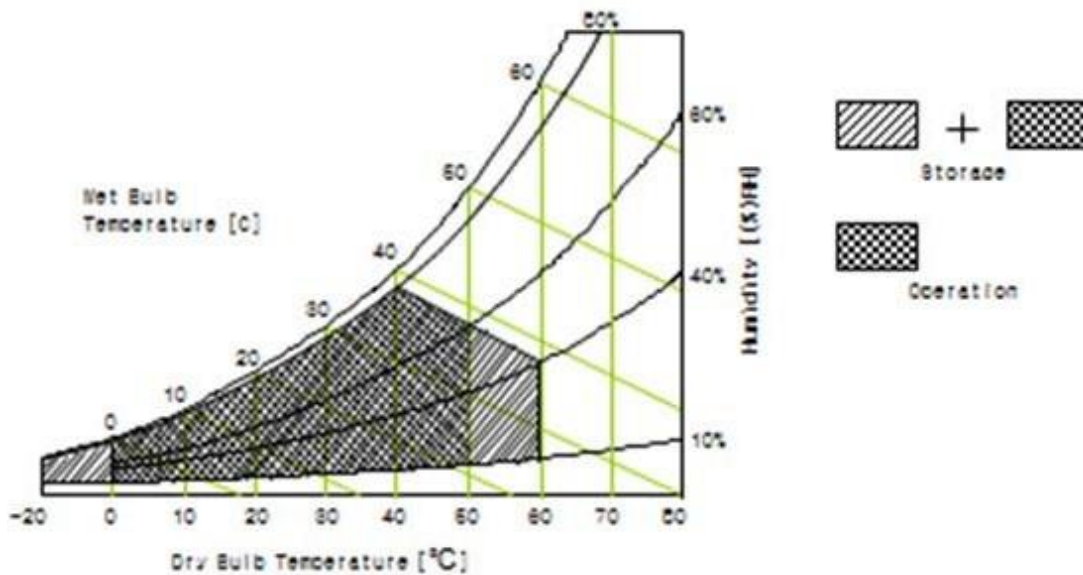
< Table 2. LCD Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.2	V	Ta = 25 °C
Operating Temperature	T _{OP}	0	+50	°C	Note 1
	T _{SUR}	0	+60	°C	
Storage Temperature	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	H _{op}	10	80	%RH	
Storage Humidity	H _{st}	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °Cmax. and no condensation of water.



3.0 Electrical Specifications

3.1 Electrical Specifications

[Ta =25±2 °C]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	V	
Power Supply Ripple Voltage		VRP			500	mV	
Power Supply Current		IDD	-	263	340	mA	Note 1
Power Consumption		PDD		3.156	4.2	W	
LVDS Interface	Differential Input High Threshold Voltage	VRTH	+100		+360	mV	
	Differential Input Low Threshold Voltage	VRTL	-360		-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

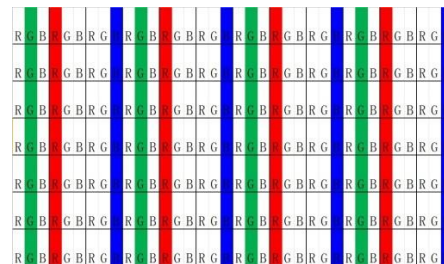
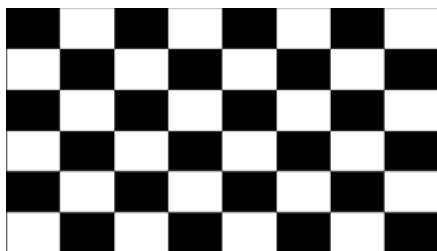
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.The current draw and power consumption specified is for VDD=12.0V, Frame rate $f_v=60\text{Hz}$ and Clock frequency = 75.4MHz.

Test Pattern of power supply current

a) Typ : Mosaic 8 x 8 Pattern*)

b) Max : Vertical Line Sub Line255

(Only display 1/3) (L0/L255)



3.2 Backlight Unit

Backlight Input Pin Assignments

Pin No.	Symbol	Feature
1	CH1+	VLED OUT CH1
2	CH1-	I Return CH1
3	NC	NC
4	NC	NC
5	CH2+	VLED OUT CH2
6	CH2-	I Return CH2

DC Input Specification

[Ta =25±2 °C]

Parameter		Min.	Typ.	Max.	Unit
LED Forward Voltage	VF	40.6	43.4	44.8	V
LED Forward Current	IF		208	240	mA
LED Power Consumption	PLED		18		W
LED Lifetime	N/A		30000		Hour

Notes: The LED Lifetime define as the estimated time to 50% degradation of initial luminous.

4.0 Interface Connection

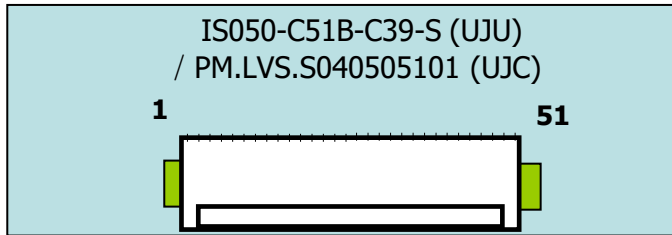
4.1 Module Input Signal & Power

Connector: S050-C51B-C39-S or Equivalent.

Pin No	Symbol	Description	Pin No	Symbol	Description
1	N.C.	No Connection	27	GND	LVDS Receiver Signal (+)
2	SDA	SDA	28	CH2_0-	LVDS Channel 2, Signal0-
3	SCL	SCL	29	CH2_0+	LVDS Channel 2, Signal0+
4	WP	Write Production	30	CH2_1-	LVDS Channel 2, Signal1-
5	N.C.	Ground	31	CH2_1+	LVDS Channel, Signal1+
6	N.C.	Ground	32	CH2_2-	LVDS Channel 2, Signal2-
7	LVDS_SEL	'H'=JEIDA, 'L' or NC= VESA	33	CH2_2+	LVDS Channel, Signal2+
8	N.C.	Ground	34	GND	Ground
9	N.C.	No Connection	35	CH2_CLK-	LVDS Channel 2, Clock-
10	GND	No Connection	36	CH2_CLK+	LVDS Channel 2, Clock+
11	GND	Ground	37	GND	Ground
12	CH1_0-	LVDS Channel 1, Signal0-	38	CH2_3-	LVDS Channel 2, Signal3-
13	CH1_0+	LVDS Channel 1, Signal0+	39	CH2_3+	LVDS Channel 2, Signal3+
14	CH1_1-	LVDS Channel 1, Signal1-	40	N.C.	No Connection
15	CH1_1+	LVDS Channel 1, Signal1+	41	N.C.	No Connection
16	CH1_2-	LVDS Channel 1, Signal2-	42	GND	Ground
17	CH1_2+	LVDS Channel 1, Signal2+	43	GND	Ground
18	GND	Ground	44	GND	Ground
19	CH1_CLK-	LVDS Channel 1, Clock-	45	GND	Ground
20	CH1_CLK+	LVDS Channel 1, Clock+	46	GND	Ground
21	GND		47	N.C.	No Connection
22	CH1_3-	LVDS Channel 1, Signal3-	48	VDD	Power Supply +12.0V
23	CH1_3+	LVDS Channel 1, Signal3+	49	VDD	Power Supply +12.0V
24	N.C.	No Connection	50	VDD	Power Supply +12.0V
25	N.C.	No Connection	51	VDD	Power Supply +12.0V
26	GND	Ground			

- Notes: 1. NC(Not Connected) : This pins are only used for internal operations.
 2. Input Level of LVDS signal is based on the EIA-644 Standard.
 3. LVDS_SEL: This pin is used for selecting LVDS signal data format.
 If this Pin: High (3.3V) → JEIDA LVDS format
 Otherwise: Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM



BIST Pattern

PT1: Black (2 sec)	PT1: White (2 sec)	PT1: Red (2 sec)	PT1: Green (2 sec)	PT1: Blue (2 sec)

Flicker Pattern

+	-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+	-	+

4.2 LVDS Interface

LVDS Receiver: Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

< Table 5. Open Cell Input Connector Pin Configuration >

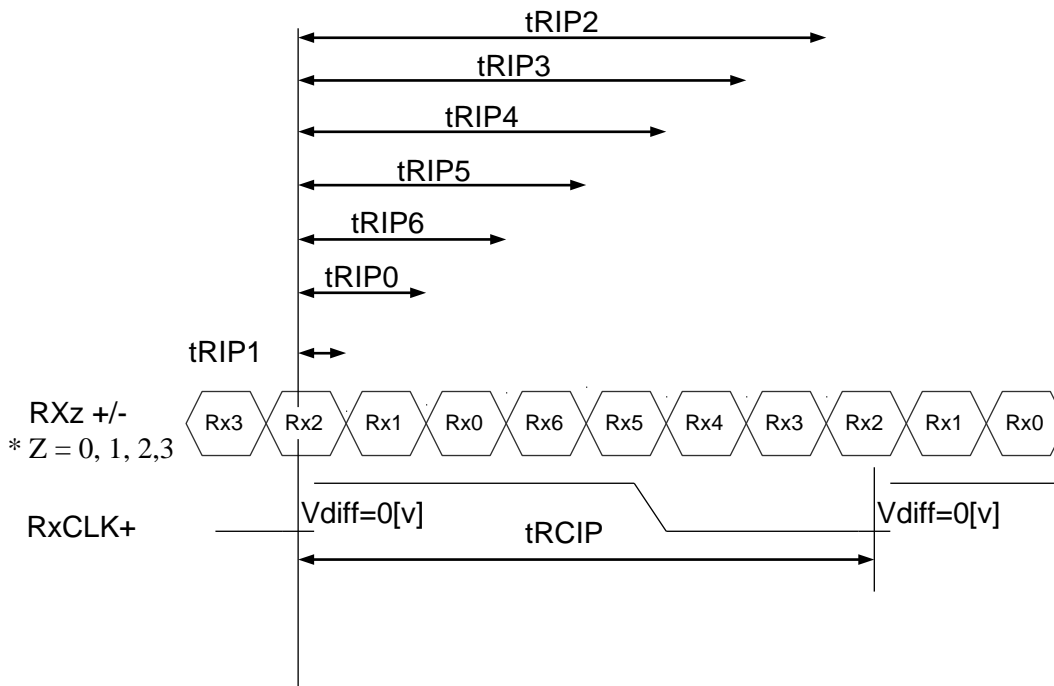
	LVDS Pin	Vesa Data format	JEIDA Data format	Remark
TxOUT/RxIN0	TxIN/RxOUT0	Red0 [LSB]	R2	
	TxIN/RxOUT1	Red1	R3	
	TxIN/RxOUT2	Red2	R4	
	TxIN/RxOUT3	Red3	R5	
	TxIN/RxOUT4	Red4	R6	
	TxIN/RxOUT6	Red5	R7 [MSB]	
	TxIN/RxOUT7	Green0 [LSB]	G2	
TxOUT/RxIN1	TxIN/RxOUT8	Green1	G3	
	TxIN/RxOUT9	Green2	G4	
	TxIN/RxOUT12	Green3	G5	
	TxIN/RxOUT13	Green4	G6	
	TxIN/RxOUT14	Green5	G7 [MSB]	
	TxIN/RxOUT15	Blue0 [LSB]	B2	
	TxIN/RxOUT18	Blue1	B3	
TxOUT/RxIN2	TxIN/RxOUT19	Blue2	B4	
	TxIN/RxOUT20	Blue3	B5	
	TxIN/RxOUT21	Blue4	B6	
	TxIN/RxOUT22	Blue5	B7 [MSB]	
	TxIN/RxOUT24	HSYNC	HSYNC	
	TxIN/RxOUT25	VSYNC	VSYNC	
	TxIN/RxOUT26	DEN	DEN	
TxOUT/RxIN3	TxIN/RxOUT27	Red6	R0 [LSB]	
	TxIN/RxOUT5	Red7 [MSB]	R1	
	TxIN/RxOUT10	Green6	G0 [LSB]	
	TxIN/RxOUT11	Green7 [MSB]	G1	
	TxIN/RxOUT16	Blue6	B0 [LSB]	
	TxIN/RxOUT17	Blue7 [MSB]	B1	
	TxIN/RxOUT23	Reserved	Reserved	

4.3 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 6. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCIP	10.20	13.47	17.08	nsec	
Input Data 0	tRIP1	-0.4	0.0	+0.4	nsec	
Input Data 1	tRIP0	tRCIP/7-0.4	tRCIP/7	tRCIP/7+0.4	nsec	
Input Data 2	tRIP6	2 ×tRCIP/7-0.4	2 ×tRCIP/7	2 ×tRCIP/7+0.4	nsec	
Input Data 3	tRIP5	3 ×tRCIP/7-0.4	3 ×tRCIP/7	3 ×tRCIP/7+0.4	nsec	
Input Data 4	tRIP4	4 ×tRCIP/7-0.4	4 ×tRCIP/7	4 ×tRCIP/7+0.4	nsec	
Input Data 5	tRIP3	5 ×tRCIP/7-0.4	5 ×tRCIP/7	5 ×tRCIP/7+0.4	nsec	
Input Data 6	tRIP2	6 ×tRCIP/7-0.4	6 ×tRCIP/7	6 ×tRCIP/7+0.4	nsec	



* Vdiff = (RXz+)-(RXz-),.....,(RXCLK+)-(RXCLK-)

5.0 Signal Timing Specification

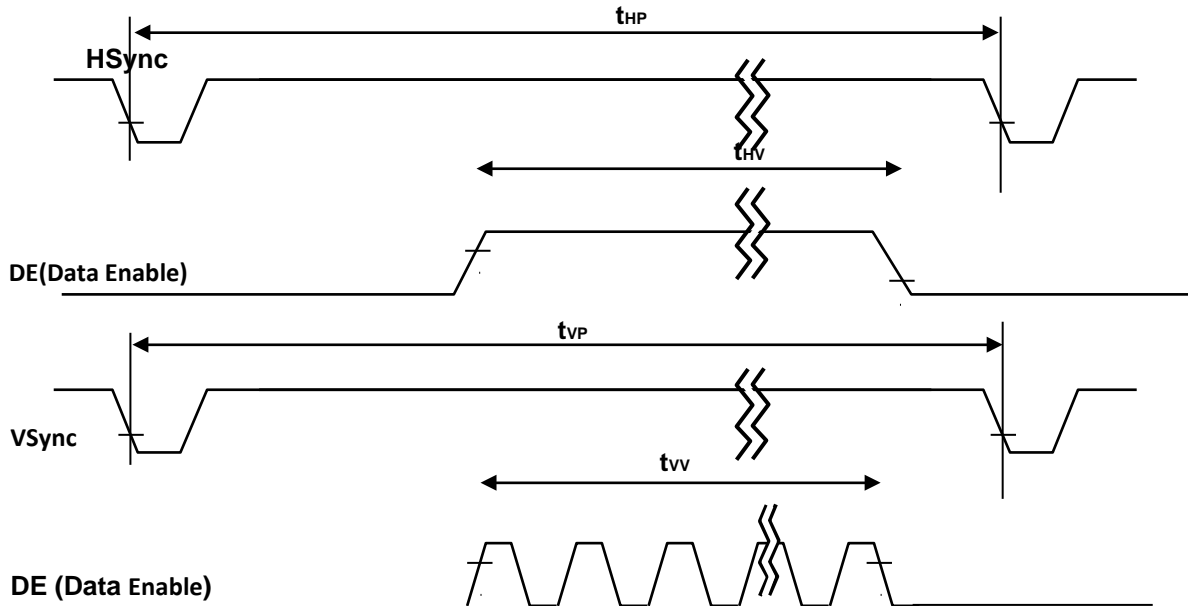
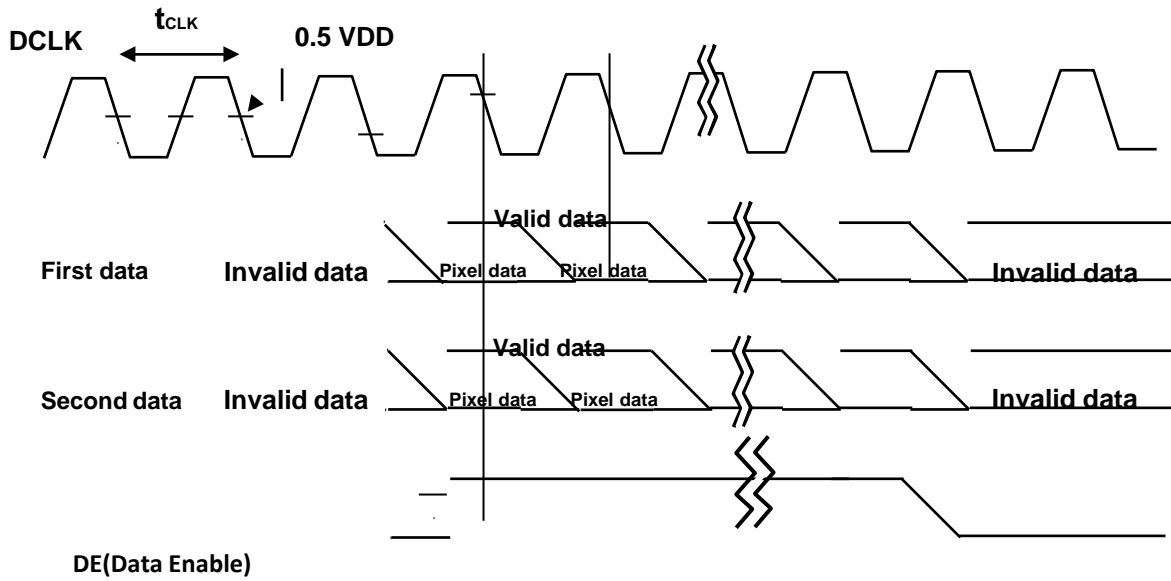
5.1 Timing Parameters (DE only mode)

< Table 7. Timing Table >

Item		Symbols	Min	Typ	Max	Unit	
Clock	Frequency	1/Tc	58	74.25	97	MHz	
	High Time	Tch	-	4/7Tc	-		
	Low Time	Tcl	-	4/7Tc	-		
Frame Period		Tv	1100	1125	1149	lines	
			47	60	78	Hz	
Horizontal Active Display Term		Valid	t _{HV}	-	960	-	t _{CLK}
		Total	t _{HP}	1060	1100	1200	t _{CLK}
Vertical Active Display Term		Valid	t _{VV}	-	1080	-	t _{HP}
		Total	t _{VP}	1100	1125	1149	t _{HP}

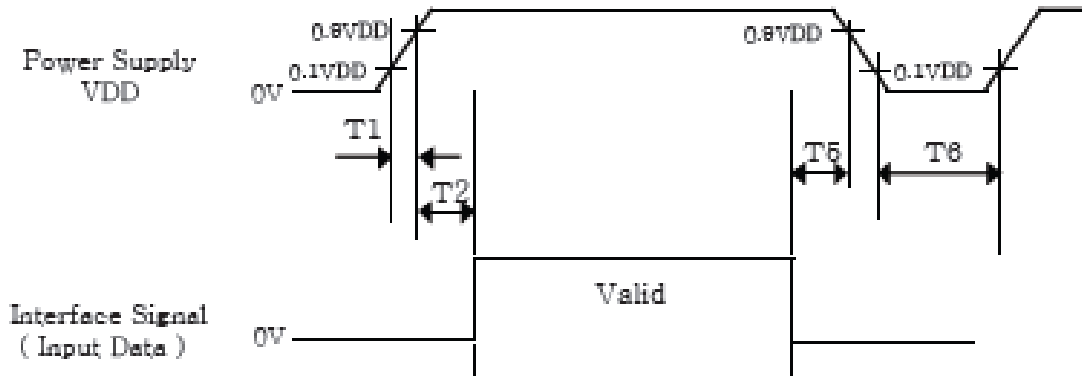
Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

5.2 Signal Timing Waveform



5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequences shall be as shown in below.



< Table 9. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	0	-	50	ms
T5	0	-	50	ms
T6	1	-	-	s

Notes: 1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.

2. Back Light must be turn on after power for logic and interface signal are valid.

6.0 Optical Specifications

The test of optical specifications shall be measured in a dark room (ambient luminance \leq 1 lux and temperature $=25\pm 2^{\circ}\text{C}$) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and ϕ equal to 0° . We refer to $\theta_{\phi=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\phi=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\phi=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\phi=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or ϕ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V

+/-10% at 25°C . Optimum viewing angle direction is 6'clock.

< Table 10. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta = $25\pm 2^{\circ}\text{C}$]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	θ_3	CR > 10		89		Deg.	Note 1
		θ_9			89		Deg.	
	Vertical	θ_{12}			89		Deg.	
		θ_6			89		Deg.	
Contrast ratio		CR			1200:1			Note 2
Luminance of White		Y_w			700		nit	Note3
White luminance uniformity		ΔY		75	80		%	Note4
Color Gamut					72		%	
Reproduction of color	White	W_x	$\theta = 0^{\circ}$ (Center) Normal Viewing Angle		0.275			Note5 YR BLU
		W_y			0.300			
	Red	R_x			0.652			
		R_y			0.331			
	Green	G_x			0.287			
		G_y			0.617			
	Blue	B_x			0.147			
		B_y			0.084			
Response Time	G to G	T_g		-	8	-	ms	Note 6
Gamma Scale				2.0	2.2	2.4		
Cell Transmittance					6.0		%	

7.0 Mechanical Characteristics

7.1 Dimensional Requirements

Figure 4 (located in Appendix) shows mechanical outlines for the model HM280FH111B.
Other parameters are shown in Table 11.

< Table 11. Dimensional Parameters >

Parameter	Specification	Unit
Dimensional outline	732(H) × 165(V)	mm
Weight	2.4	Kg
Active area	699.84(H) × 131.22(V)	mm
Pixel pitch	121.5 × 364.5	um
Number of pixels	1920(H) × 360(V)	pixels

8.0 Reliability Test Condition

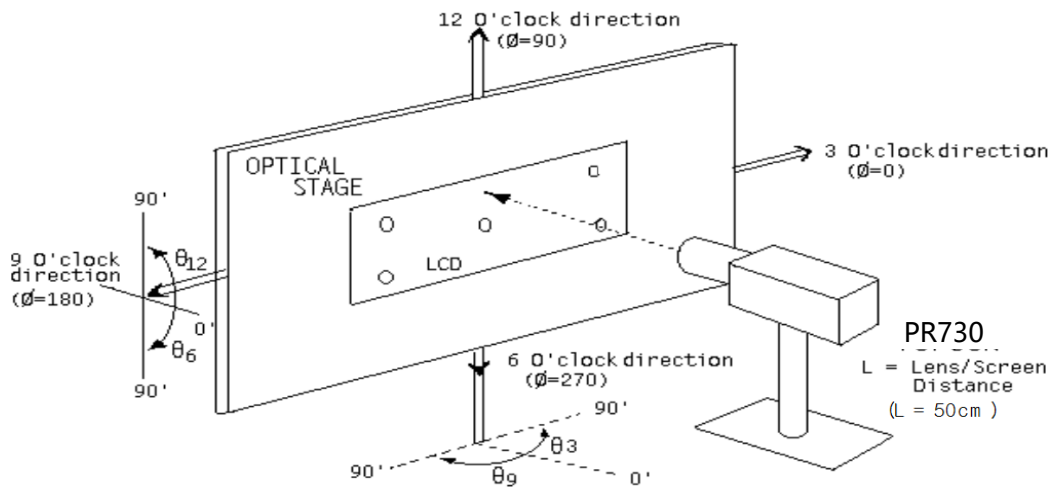
Item	Test Condition
High-Temp/OP	Ta = 60 °C, 240 hrs
Low-Temp/OP	Ta = 0 °C, 240 hrs
Low-Temp/STG	Ta = -20 °C, 240hrs
On/Off	30sec(on) / 30sec(off) , 12000times, 200hr
TST-2	-40°C~80°C (Per 30min) , 100 cycle
Altitude	First 5000ft After 15000ft; 0°C/24hr; 25°C/24hr; 50°C/24hr
ESD	Front/Left @ Center≤18dB, Rear/Inverter≤25dB 150pF 330Ω ±15KV(Air) / ±8kV (Contact), 100point
Module VIB	Random: +X/+Y/+Z(30min) ; 1.5G; 10~500HZ
Shock	50G 11msec ; Half sine; ±X±Y±Z axis

This test condition is based on module.

9.0 Appendix

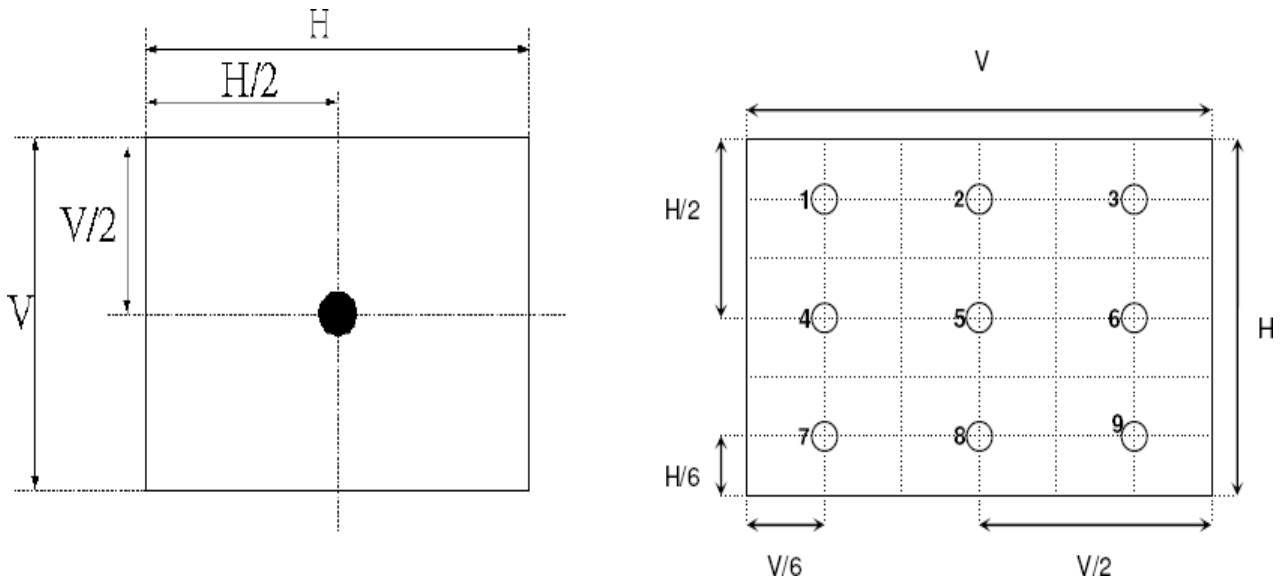
(I)

< Figure 1. Measurement Set Up >



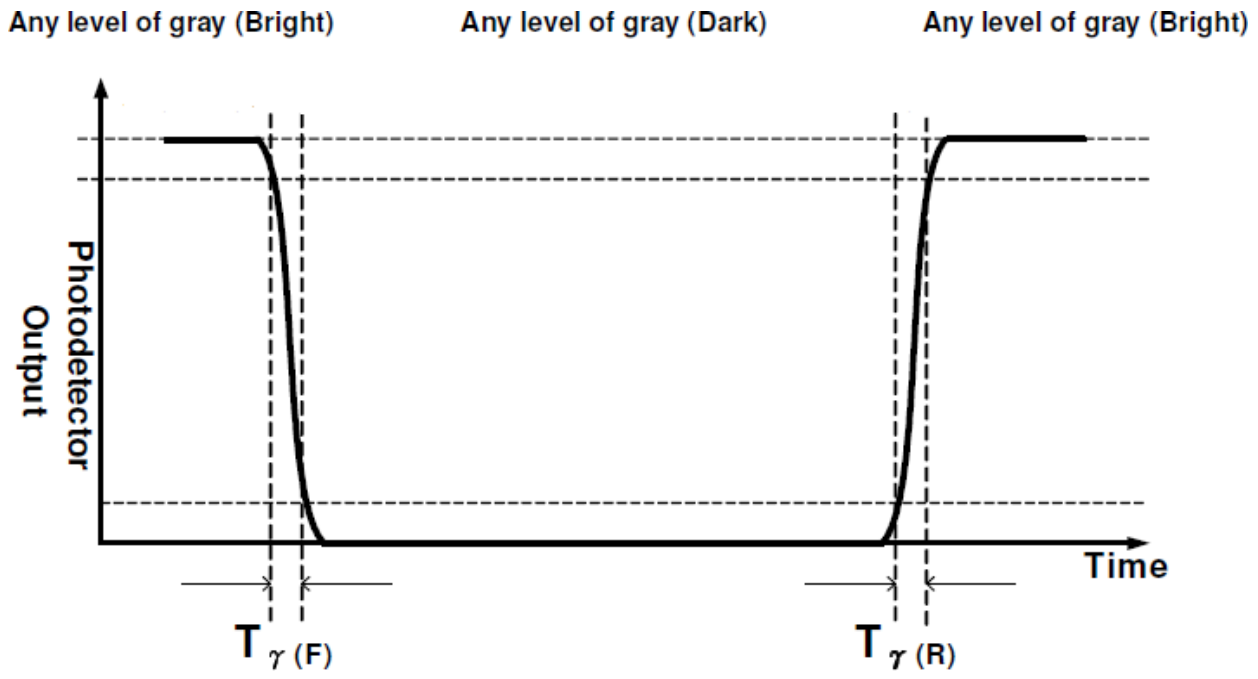
(II)

< Figure 2. White Luminance and Uniformity Measurement Locations >

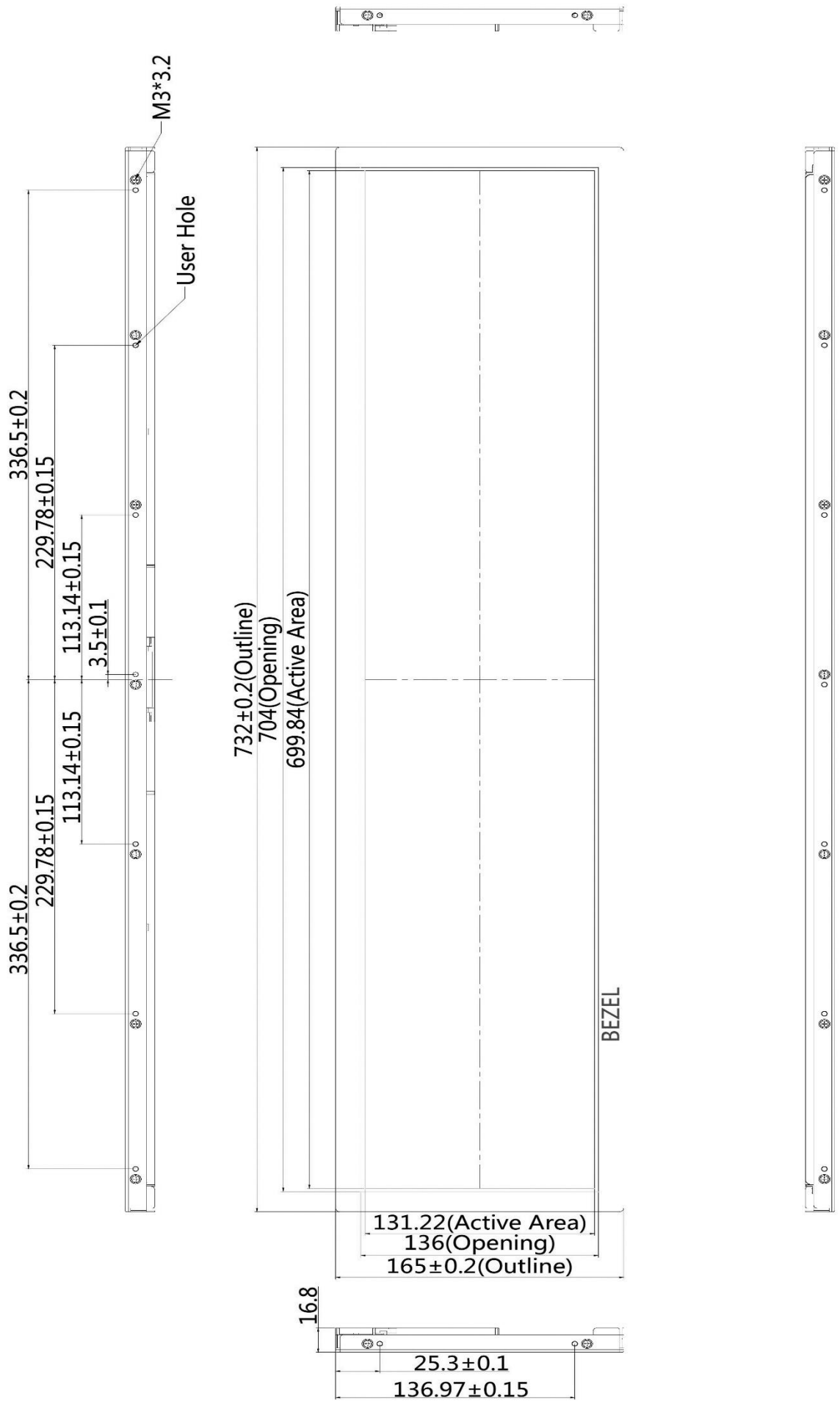


(III)

< Figure 2. Response Time Testing >



< Figure 3. TFT-LCD Module Outline Dimensions (Front View) >



< Figure 4. TFT-LCD Module Outline Dimensions (Rear View) >

