HM084SV101IV

8.4" Color TFT-LCD

FUNCTIONAL DRAFT SPECIFICATION

(This document is meant for customers' approval)

Release Date
15th Jun 2020

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1.0 General Descriptions

1.1 Introduction

The HM084SV101IV is a Color Active Matrix Liquid Crystal Display with a back-light system. The matrix employs a-Si Thin Film Transistor as a switching device. This TFT LCD has a 8.4 inch diagonally measured active display area with SVGA resolution (800 horizontal by 600 vertical pixels array).

1.2 Features

- ■ Supported SVGA Resolution
- ■ LVDS Interface
- ■ Compatible with RoHS Standard

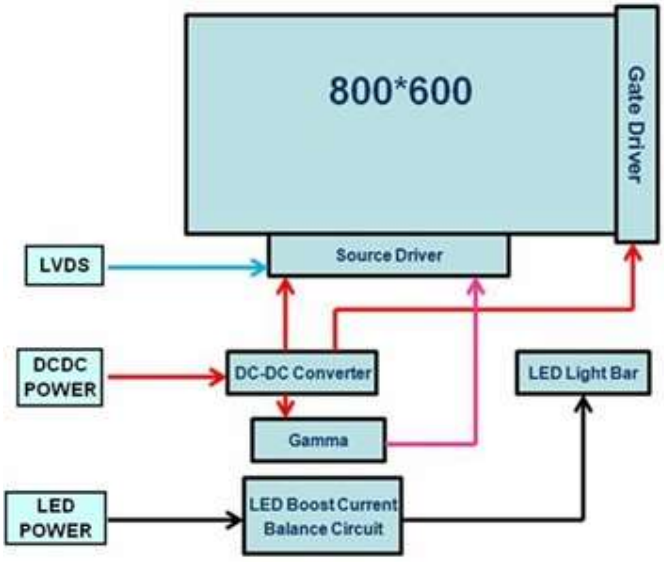
1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	8.4	inch
Active Area (H x V)	170.4(H) x127.8(V)	mm
Number of Pixels (H x V)	800x 600	-
Pixel Pitch (H x V)	0.213 x 0.213	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White	-
White Luminance	(350) (Typ.)	cd /m^2
Contrast Ratio	(600) (Typ.)	-
Response Time	(16)(Typ.)	ms
Input Voltage	3.3 (Typ.)	V
Power Consumption	(2.81)(Max)	W
Weight	(200) (Typ)	g
Outline Dimension (H x V x D)	(203. 0) (Typ.) x (142.5) (Typ.) x (5.7)(Typ.)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	262 K/16.7 M	-
NTSC	(45)(Typ.)	%
Viewing Direction	12 O'clock	-
Surface Treatment	Anti-glare	-

1.4 Functional Block Diagram

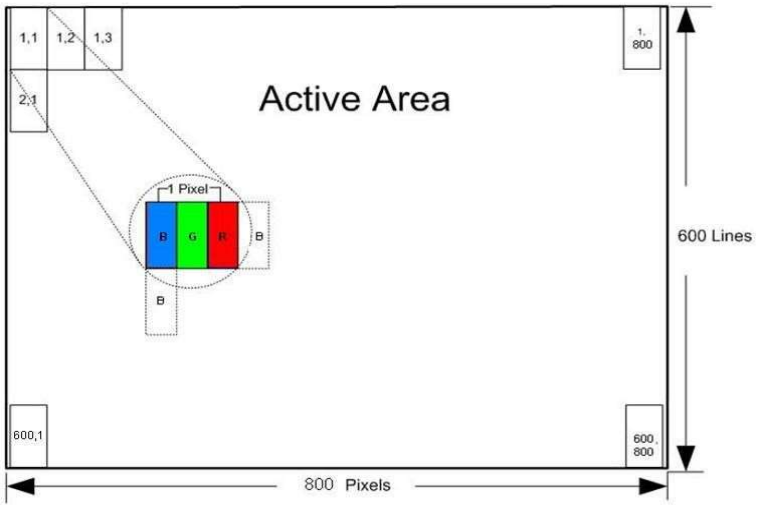
Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram



1.5 Pixel Mapping

Figure2 Pixel Mapping



2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	2.5	3.6	V	(1),(2) (3),(4)
Logic Input Signal Voltage	V_{Signal}	0	3.6	V	
Operating Temperature	T_{gs}	-20	70	℃	
Storage Temperature	T_a	-30	80	℃	

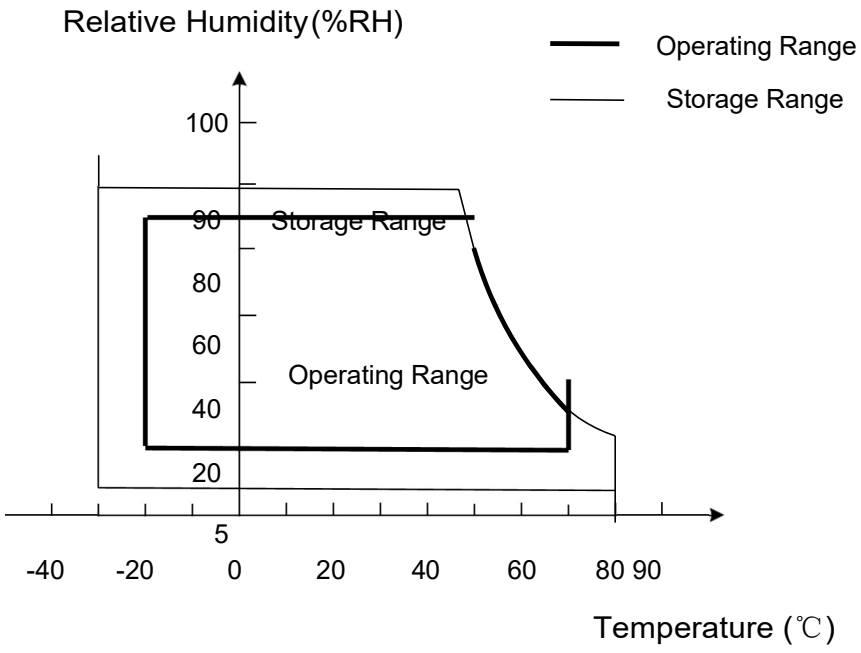
Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. I t is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 39℃, and no condensation of water. Besides, protect the module from static electricity.

Figure 3 Absolute Ratings of Environment of the LCD Module



3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

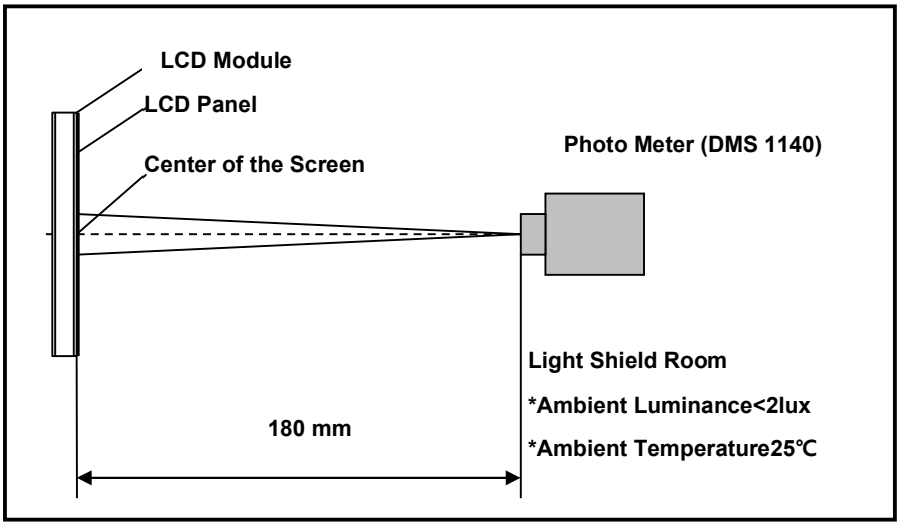
Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR>10）	Horizontal	θ_{x+}	(70)	(80)	-	degree	(1),(2),(3),(8)
		θ_{x-}	(70)	(80)	-		
	Vertical	θ_{y+}	(70)	(80)	-		
		θ_{y-}	(50)	(60)	-		
Contrast Ratio	Center		(480)	(600)	-	-	(1),(2),(4),(8) θx=θy=0°
Response Time	Rising + Falling		-	(16)	(25)	ms	(1),(2),(5),(8) θx=θy=0°
Color Chromaticity (CIE1931)	Red x		Typ -(0.03)	(0.603)	Typ +(0.03)	-	(1),(2),(3),(8) θx=θy=0°
	Red y			(0.336)		-	
	Green x			(0.326)		-	
	Green y			(0.546)		-	
	Blue x			(0.159)		-	
	Blue y			(0.110)		-	
	White x		(0.26)	(0.310)	(0.36)	-	
	White y		(0.28)	(0.330)	(0.38)	-	
NTSC	-		(42)	(45)	-	%	(1),(2),(3),(8) θx=θy=0°
White Luminance	Center point		(280)	(350)	-	cd/m^2	(1),(2) θx=θy=0°
Luminance Uniformity	9 Points		(70)	(75)	-	%	(1),(2),(6) θx=θy=0°

Note (1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature(25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

Figure 4 Measurement Setup



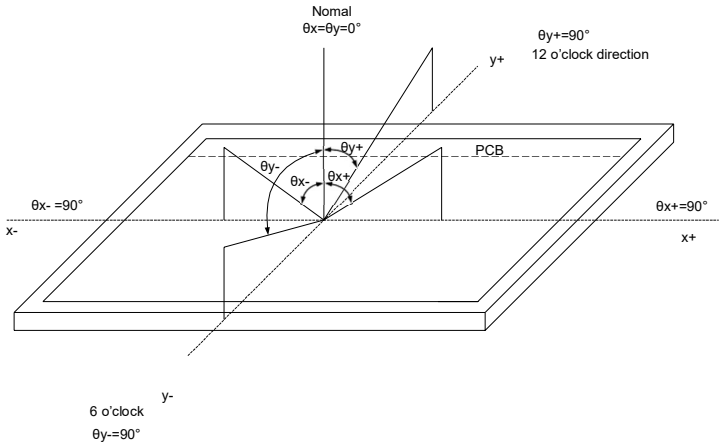
Note (2) The LED input parameter setting as:

I_LED: 68mA

PWM_LED: Duty 100 %

Note (3) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (4) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

6bit: Contrast Ratio (CR) = L63 / L0

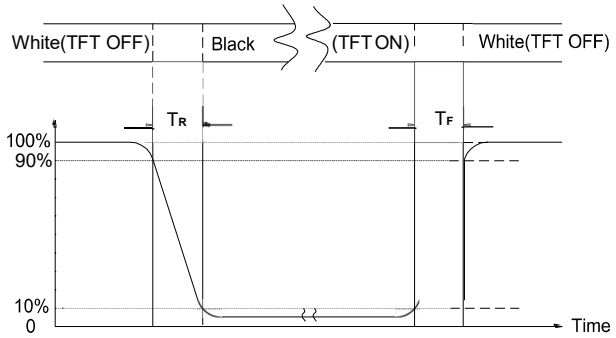
L63: Luminance of gray level 63, L0: Luminance of gray level 0

8bit: Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (5) Definition of Response Time (T_R, T_F)

Figure 6 Definition of Response Time



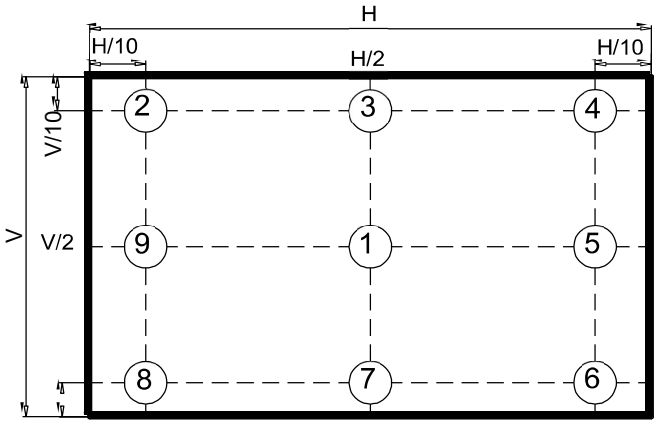
Note (6) Definition of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of gray level 255 at 9 points.

Luminance Uniformity= Min.(L1, L2, ... L9) / Max.(L1, L2, ... L9)

H—Active Area Width, V—Active Area Height, L—Luminance

Figure 7 Measurement Locations of 9 Points



V/10

Note (7) Definition Of Luminance Uniformity (Ref.: Active Area)
Measure the luminance of gray level 255 at 9 points.
Luminance Uniformity= Min.(L1, L2, ... L9) / Max.(L1, L2, ... L9)
H—Active Area Width, V—Active Area Height, L—Luminance

Note (8) All optical data based on HIGHNESS given system & nominal parameter & testing machine in this document.

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
LVDS Connector	MSB24013P20
LED Driver Connector	MSB24038P4

Table 4-1 LVDS&POWER Connector Pin Assignment

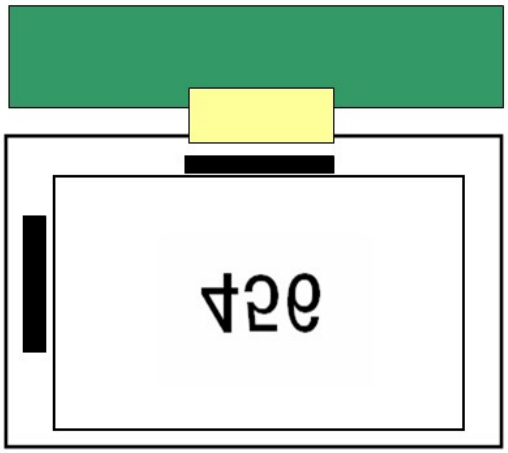
Pin No.	Symbol	Description	Remarks
1	VDD	Power Supply, 3.3V (typical)	-
2	VDD	Power Supply, 3.3V (typical)	-
3	UD	Vertical Reverse Scan control.	(1)(2)(3)(4)
4	LR	Horizontal Reverse Scan control	
5	RxIN1-	-LVDS differential data input (R0-R5,G0)	-
6	RxIN1+	+LVDS differential data input (R0-R5,G0)	-
7	GND	Ground	-
8	RxIN2-	-LVDS differential data input (G1-G5,B0-B1)	-
9	RxIN2+	+LVDS differential data input (G1-G5,B0-B1)	-
10	GND	Ground	-
11	RxIN3-	-LVDS differential data input (B2-B5,HS,VS,DE)	-
12	RxIN3+	+LVDS differential data input (B2-B5,HS,VS,DE)	-
13	GND	Ground	-
14	RxCLKIN-	-LVDS differential clock input	-
15	RxCLKIN+	+LVDS differential clock input	-
16	GND	Ground	-
17	SEL68	6/8 bits LVDS data input selection(H:8bit L/NC:6bit)	VH:2.5V-3.6V
18	BIST	H:BIST MODE, L/NC: Normal MODE	VL:0V-0.5V

19	RxIN4-	-LVDS differential data input (R6-R7,G6-G7,B6-B7)	-
20	RxIN4+	+LVDS differential data input (R6-R7,G6-G7,B6-B7)	-

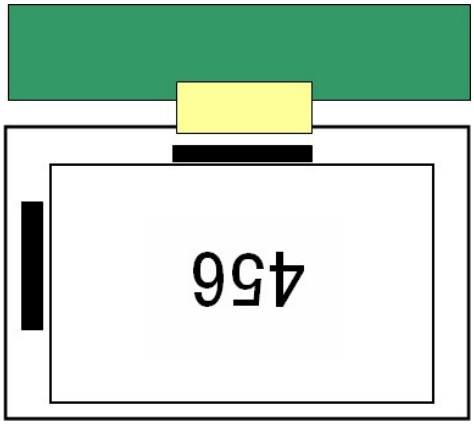
Table 4-2 LED Driver Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	VLED	LED Driver Power Supply, 12V (typical)	-
2	GND	Ground	-
3	EN	LED Driver Enable	VH:2.5V-6V
4	PWM	PWM Signal input	VL:0V-0.5V

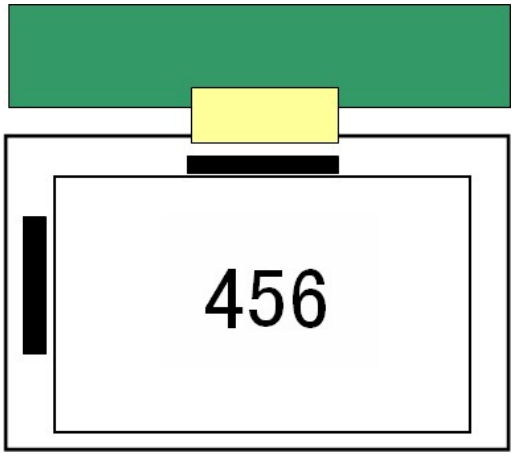
(1) UD= HIGH(VH:2.5V-3.6V),LR=LOW(VL:0V-0.5V)



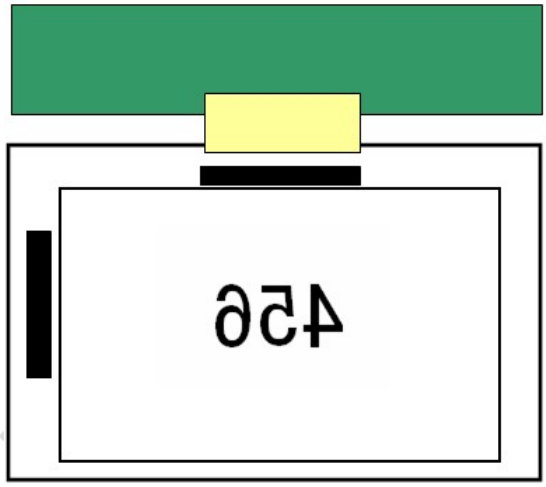
(2) UD= HIGH(VH:2.5V-3.6V),LR=HIGH(VH:2.5V-3.6V)



(3) UD= LOW(VL:0V-0.5V),LR=LOW(VL:0V-0.5V)



(4) UD= LOW(VL:0V-0.5V),LR=HIGH(VH:2.5V-3.6V)



4.2 Signal Electrical Characteristics

4.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 5 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	V_{CM}=+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	V_{CM}=+1.2V
Magnitude Differential Input Voltage	$\|V_{ID}\|$	200	-	600	mV	-
Common Mode Voltage	V_{CM}	$\|V_{ID}\|/2$	1.2	1.4	V	V_{th}-V_{tl}=200mV
Common Mode Voltage Offset	ΔV_{CM}	-50	-	+50	mV	V_{th}-V_{tl}=200mV

Note (1) Input signals shall be low or Hi- resistance state when VDD is off.

Note (2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Figure 8 Voltage Definitions

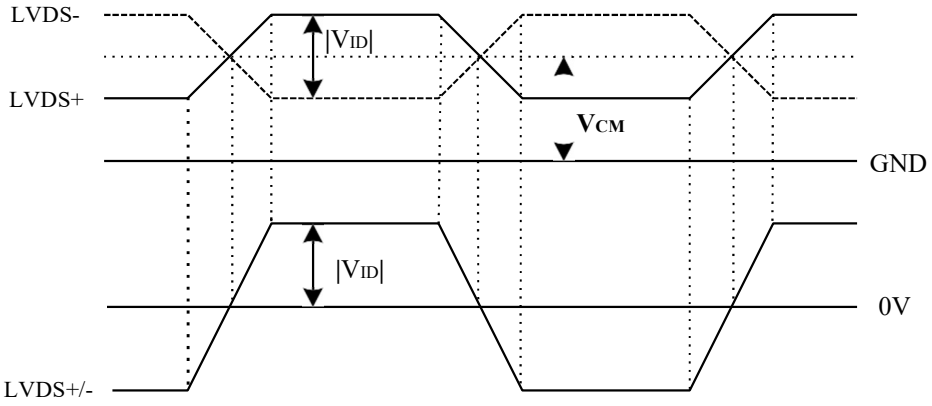


Figure 9 Measurement System

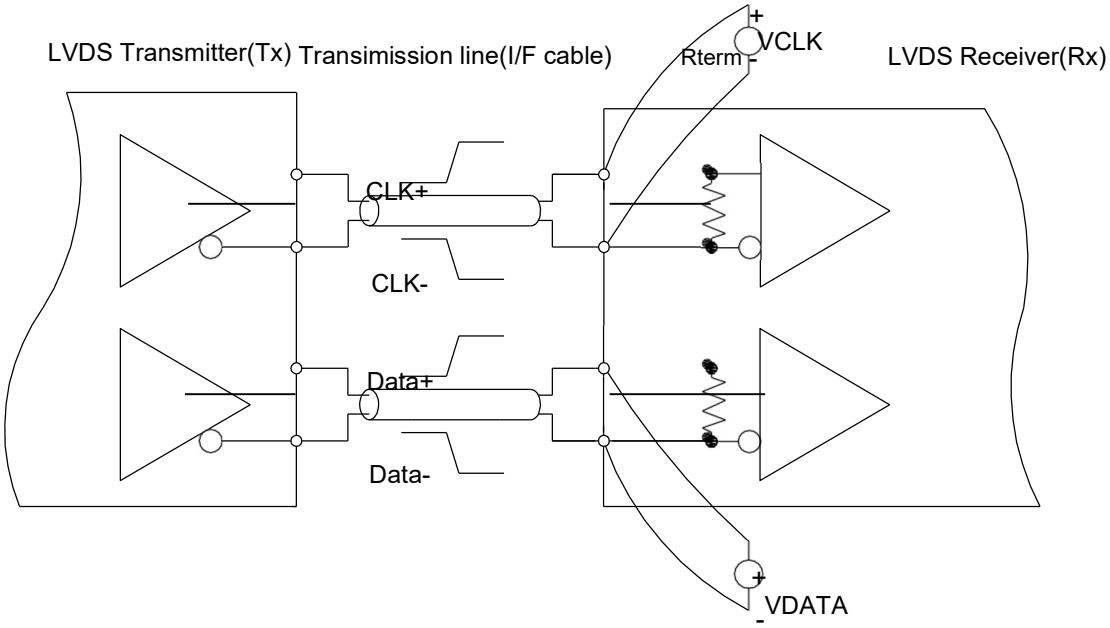
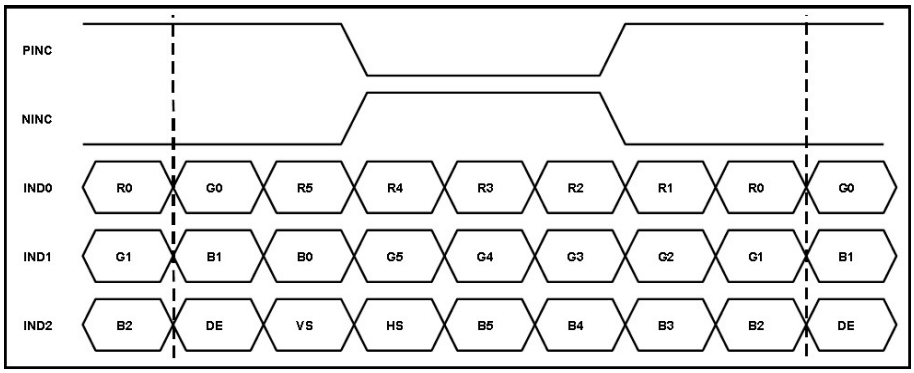
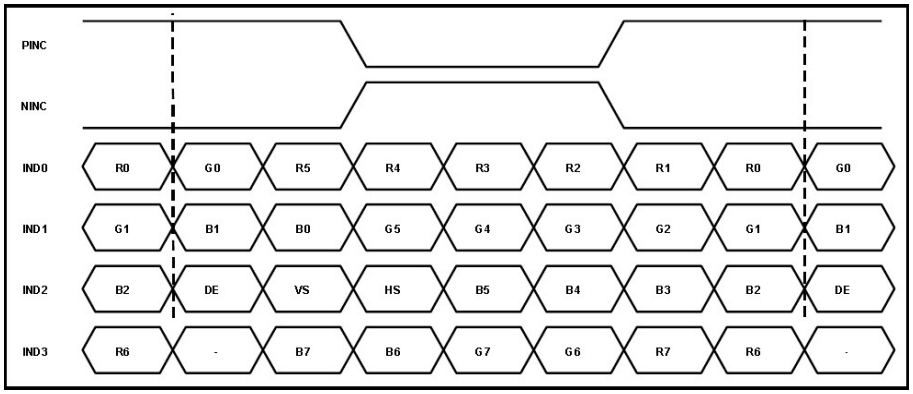


Figure 10 Data Mapping

Single 6 bit LVDS input



Single 8 bit LVDS input

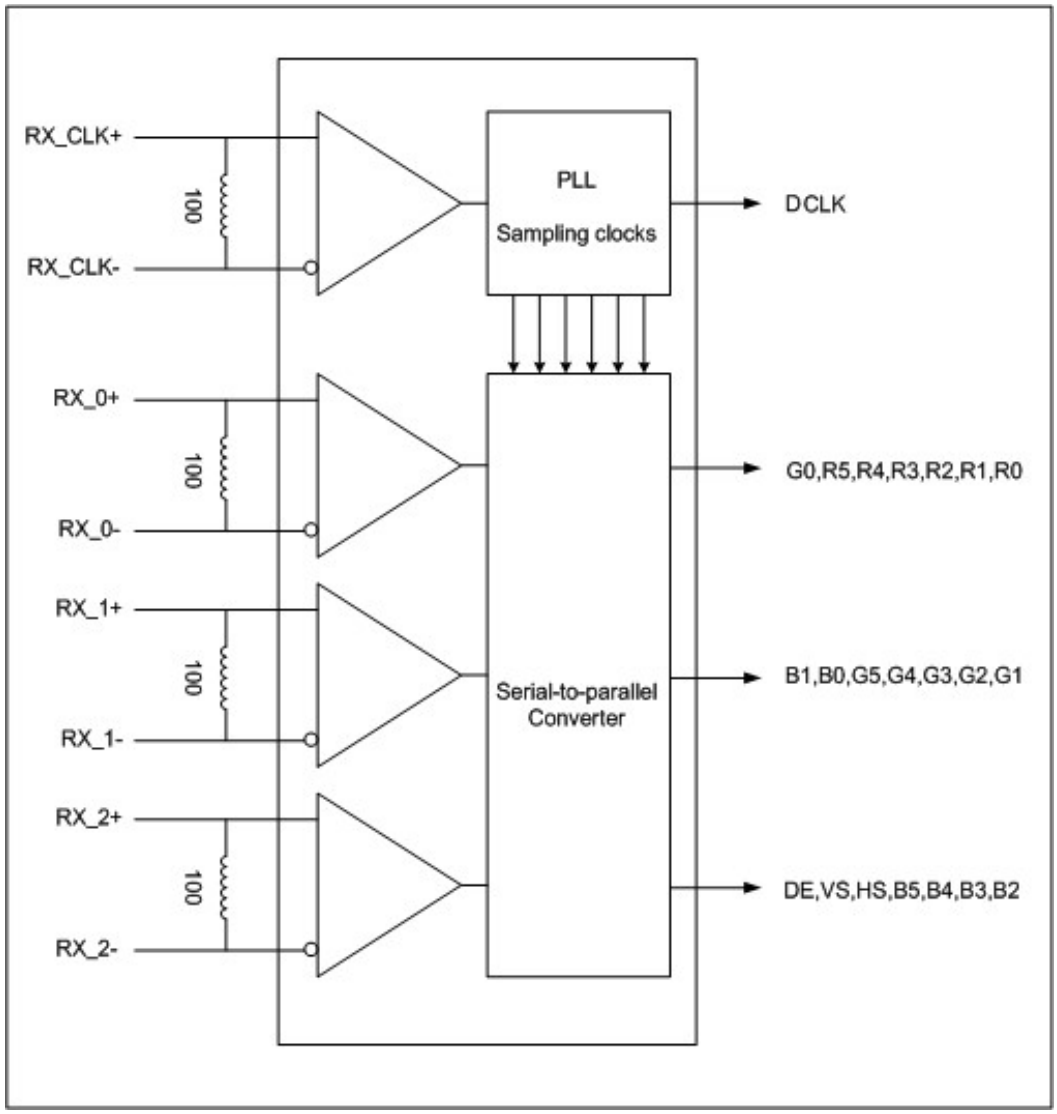


4.2.2 LVDS Receiver Internal Circuit

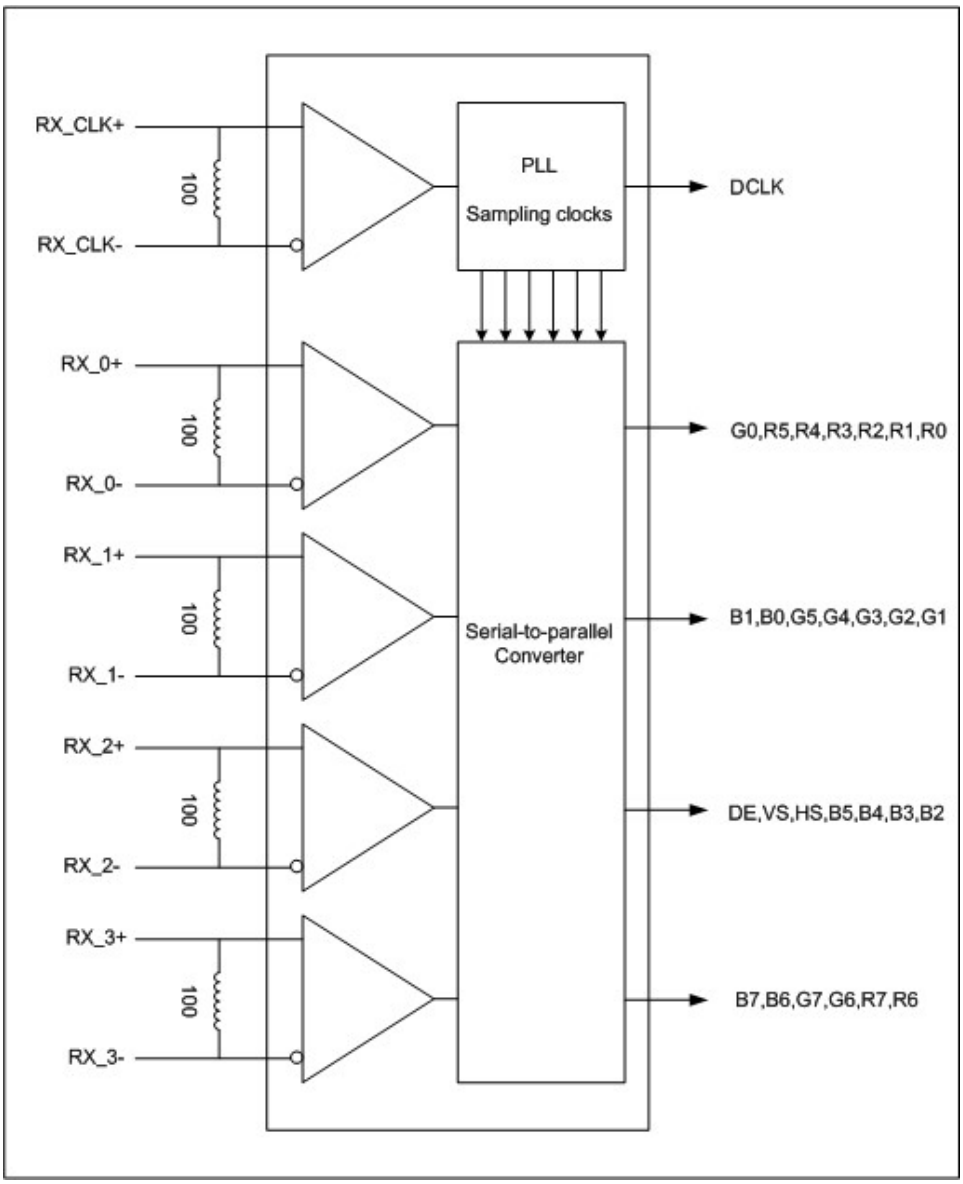
Figure 11 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 11 LVDS Receiver Internal Circuit

6bit



8bit


RX_CLK+
RX_CLK-
100
PLL
Sampling clocks
DCLK
RX_0+
RX_0-
RX_1+
RX_1-
RX_2+
RX_2-
RX_3+
RX_3-
Serial-to-parallel
Converter
G0,R5,R4,R3,R2,R1,R0
B1,B0,G5,G4,G3,G2,G1
DE,VS,HS,B5,B4,B3,B2
B7,B6,G7,G6,R7,R6

4.3 Interface Timings

Table 6 Interface Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
LVDS Clock Frequency	Fclk	32.6	39.6	62.4	MHz
H Total Time	HT	890	1000	1300	Clocks
H Active Time	HA	800	800	800	Clocks
V Total Time	VT	610	660	800	Lines
V Active Time	VA	600	600	600	Lines
Frame Rate	FV	55	60	65	Hz

Note：Htotal*Vtotal*Frame Rate＜67.6MHz

4.4 Input Power Specifications

Input power specifications are as follows.

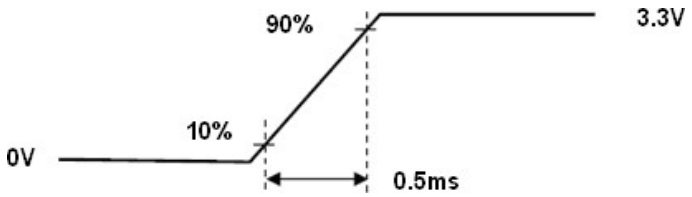
Table 7 Input Power Specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
System Power Supply							
LCD Drive Voltage (Logic)		V_{DD}	3.0	3.3	3.6	V	(1),(2),(3)
VDD Current	black Pattern	I_{DD}	-	-	(0.139)	A	(1),(4)
VDD Power Consumption	black Pattern	P_{DD}	-	-	(0.5)	W	
Rush Current		I_{Rush}	-	-	2	A	(1)(5)
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	-	200	mV	(1)
LED Power Supply							
LED Input Voltage		V_{LED}	10.8	12	13.2	V	(1),(2),(10)
LED Power Consumption		P_{LED}	-	-	(2.31)	W	(1),(6),(10)
LED Forward Voltage		V_F	2.8	3.3	3.6	V	(1), (2)
LED Forward Current		I_F	-	17	-	mA	
PWM Signal Voltage	High	V_{PWM}	(2.5)	-	(6)	V	
	Low		0	-	0.5		
LED Enable Voltage	High	V_{LED_EN}	(2.5)	-	(6)	V	
	Low		0	-	0.5		
Input PWM Frequency		F_{PWM}	100	-	2,0000	Hz	(1),(2),(7)
Duty Ratio		PWM	5	-	100	%	(1), (8)

LED Life Time	LT	(30,000)	(50,000)	-	Hours	(1)(9)

Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Figure 12 VDD Rising Time

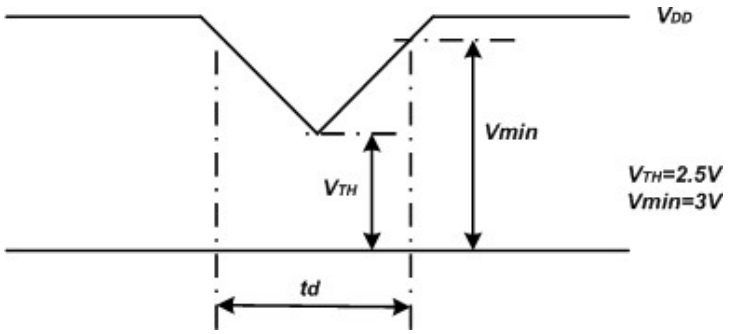


Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note (3) VDD Power Dip Condition V_{TH}< V_{DD}≤ Vmin, td≤ 10ms (a time of the voltage return to normal), our panel can recover automatically.Note (4) The specified V_{DD} current and power consumption are measured under the V_{DD} = 3.3 V,

F_V = 60 Hz condition and Black pattern.

Figure 13 VDD Power Dip



Note (5) The figures below are the measuring condition of V_{DD} and the measuring circuit that HIGHNESS display used. Rush current can be measured when T_{RUSH} is 0.5 ms.

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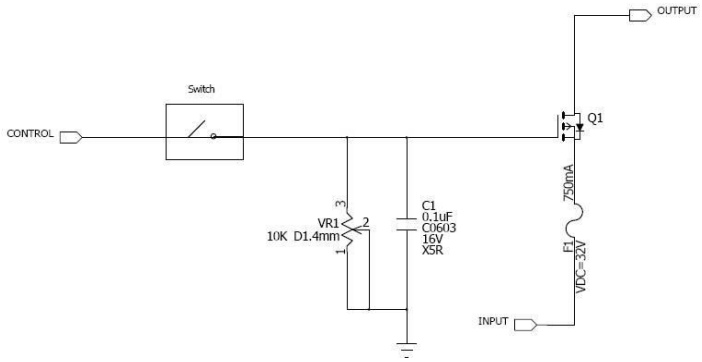
Figure 14 measuring circuit of V_{DD}



Note (6) The power consumption of LED Driver are under the V_{LED} = 12.0V, Dimming of Max luminance.

Note (7) Although acceptable range as defined, the dimming ratio is not effective at all conditions. The PWM frequency should be fixed and stable for more consistent luminance control at any specific level desired.

Note (8) The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.

Note (9) The life time is determined as the sum of the lighting time till the luminance of LCD at the typical LED current reducing to 50% of the minimum value under normal operating condition.

4.5 Power ON/OFF Sequence

Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD voltage is off.

Figure 15 Power Sequence

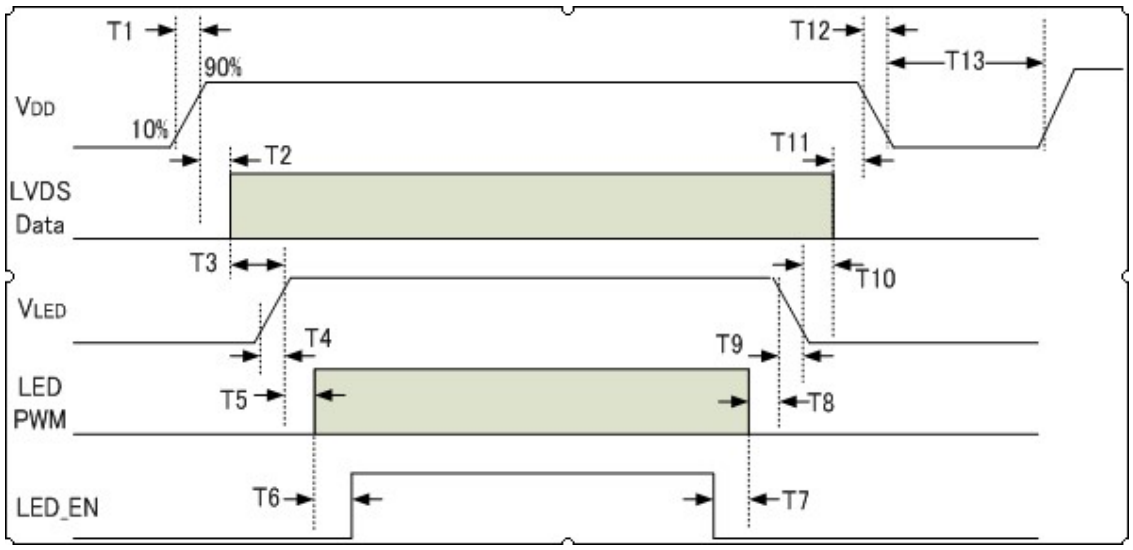


Table 8 Power Sequencing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
VIN Rise Time	T1	0.5	-	10	ms
VIN Good to Signal Valid	T2	30	-	90	ms
Signal Valid to Backlight On	T3	200	-	-	ms
Backlight Power On Time	T4	0.5	-	-	ms
Backlight VDD Good to System PWM On	T5	10	-	-	ms
System PWM ON to Backlight Enable ON	T6	10	-	-	ms
Backlight Enable Off to System PWM Off	T7	0	-	-	ms
System PWM Off to B/L Power Disable	T8	10	-	-	ms
Backlight Power Off Time	T9	1	10	30	ms
Backlight Off to Signal Disable	T10	200	-	-	ms
Signal Disable to Power Down	T11	0	-	50	ms
VIN Fall Time	T12	1	10	30	ms
Power Off	T13	500	-	-	ms

5.0 Mechanical Characteristics

5.1 Outline Drawing

Figure 16 Outline Drawing (Front Side)

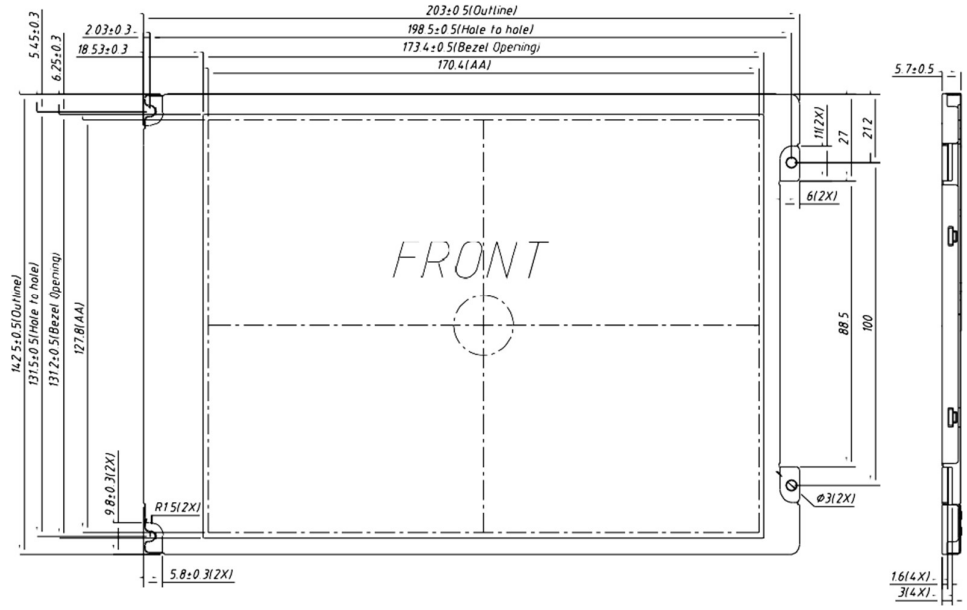


Figure 17 Reference Outline Drawing (Back Side)

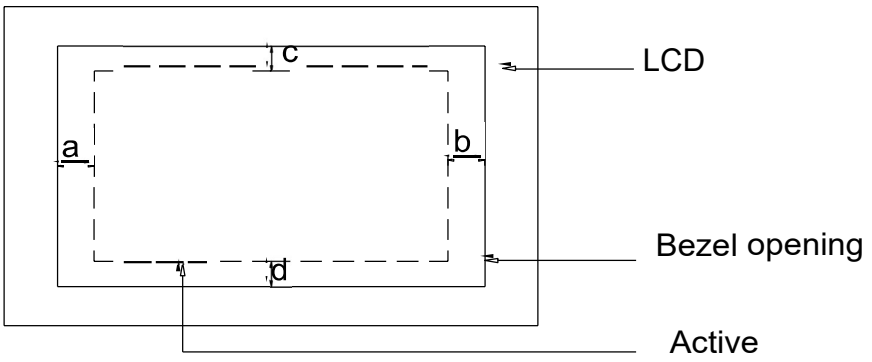
Note (1) Unnoted tolerance: ± 0.5mm.

5.2 Dimension Specifications

Table 9 Module Dimension Specifications

Item	Min.	Typ.	Max.	Unit
Width	(202.5)	(203)	(203.5)	mm
Height	(142)	(142.5)	(143)	mm
Thickness（with PCBA）	(5.2)	(5.7)	(6.2)	mm
Weight	-	(200)	(220)	g
BM:｜a-b｜&｜c-d｜	-	-	1.0	mm

Figure 18 BM Area



6.0 Reliability Conditions

Item		Package	Test Conditions		Note
Low Temperature Operating Test		Module	T_a= -20℃, 300 hours		(1),(2),(3),(4)
High Temperature Operating Test		Module	T_{gs}= 70℃, 300 hours		
High Temperature/High Humidity Operating Test		Module	T_{gs}= 50℃, 85%RH, 300 hours		
High Temperature Storage Test		Module	T_a= 80℃, 300 hours		(1),(3),(4)
Low Temperature Storage Test		Module	T_a= -30℃, 300 hours		
Shock Non-operating Test		Module	100G,6ms,X Y Z×2faces×3times, Total 18 times		(1) (3) (5)
Vibration Non-operating Test		Module	half-sine Frequency: 8Hz ~ 33Hz Stroke: 1.3mm Sweep: 2.9G 33.3Hz ~ 400Hz X,Z Cycle : 15 minutes 2 hrs for each direction of X,Z ; 4 hours for Y direction		
ESD Test	Operating	Module	Contact	± 8 KV, 150pF(330Ohm)	(1),(2),(6)
			Air	± 15 KV, 150pF(330Ohm)	
	Non-operating		Contact	± 10 KV, 150pF(330Ohm)	
			Air	± 20 KV, 150pF(330Ohm)	

Note (1) A sample can only have one test. Outward appearance, image quality and optical datacan only be checked at normal conditions according to the HIGHNESS document before reliable test. Only check the function of the module after reliability test.
Note (2) The setting of electrical parameters should follow the typical value before reliability test.
Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static.
Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. T_A= Ambient Temperature, T_{GS}=

Glass Surface Temperature.

Note (5) The module should be fixed firmly in order to avoid twisting and bending.

Note (6) It could be regarded as pass, when the module recovers from function fault caused by ESD after resetting.

Note (7) Image Sticking test should follow HIGHNESS recommend setting-voltage: Gamma, VGH, VGL, AVDD etc. Before the test, V_{com} must be adjusted to optimize display quality.

7.0 Display Label