



**HIGHNESS<sup>TM</sup>**

*One of a kind*

**HM040HD111TV**

**4.0" Circular Display**



Release Date  
09<sup>th</sup> Jun 2023

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**HIGHNESS MICROELECTRONICS PVT. LTD**

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## 1. General specification

<b>Item</b>	<b>Description</b>	<b>Unit</b>
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	720(H) x 720(V)	Dots
Color	16.7M	-
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.141(H) x 0.141(V)	mm
Active area	101.52(H) x 101.52(V)	mm
Viewing direction	ALL O'CLOCK	-
TFT Driver IC	NV3052CGRB	
TFT interface	24bit RGB	-
Approx. Weight	TBD	g
LCM Size(W*H*T)	105.6(W) x 109.87(H) x 2.13(T)	mm

## 2. Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T <sub>OPR</sub>	-20	+70	°C
LCM Storage Temperature	T <sub>STG</sub>	-30	+80	°C
Humidity	RH	-	90	%

## 3. Electrical Characteristics

### 3.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VDDIO	--	--	--	V
Supply Voltage for(DC/DC)	VDD	2.7	3.3	3.6	V
Current Consumption	I <sub>DD</sub>	--	100	--	mA
	I <sub>DD-SLEEP</sub>	--	150	--	uA

### 3.2 Back-Light Unit Characteristics

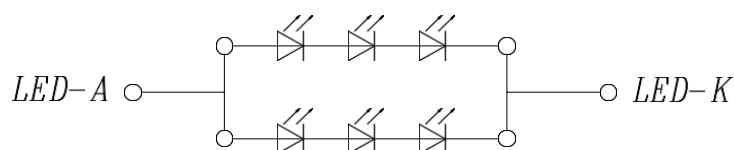
The back-light system is an edge-lighting type with 6 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V <sub>F</sub>	16.8		19.2	V	-
Forward current	I <sub>F</sub>	--	40	-	mA	-
Luminance(With LCD+CTP)	L <sub>V</sub>	--	600	--	cd/m <sup>2</sup>	-
LED life time	N/A	----	30,000	--	Hr	Note 1

Note:

- (1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I<sub>L</sub>=20mA/LED. The LED life time could be decreased if operating I<sub>L</sub> is larger than 25mA/LED.

Backlight circuit diagram shown in below:



## 4. Module Function Description

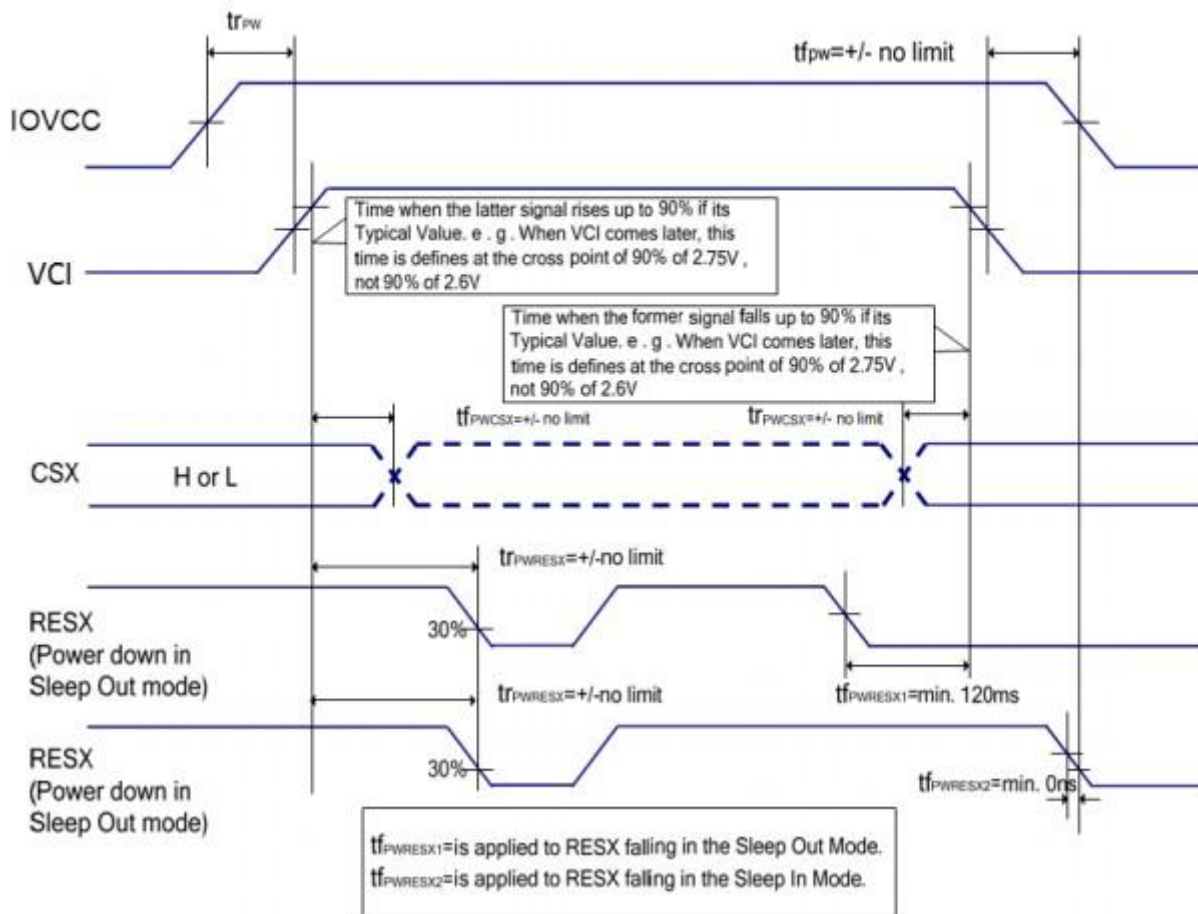
Pin No.	Symbol	Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK	Power supply for backlight cathode input terminal.	
3	VCC(3.3V)	Power Supply For LCD.	
4	GND	Power Ground	
5	GND	Power Ground	
6	DEN	Data enable signal for RGB interface operation.	
7	VSYNC	Frame synchronous signal for RGB interface operation.	
8	HSYNC	Line synchronous signal for RGB interface operation.	
9	CLK	MIPI-DSI CLOCK differential signal input pins	
10~17	B7~B0	Blue data	
18~25	G7~G0	Green data	
26~33	R7~R0	Red data	
34	RESET	Reset pin. Setting either pin low initializes the LSI	
35	CS	Chip selection signal.	
36	SCL	Serial clock signal pin.	
37	SDA	Serial data input/output pin.	
38	GND	Power Ground	
39	VCC(3.3V)	Power Supply For LCD.	
40	GND	Power Ground	

## 5. Timing Characteristics

### Power On/Off Sequence

#### Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



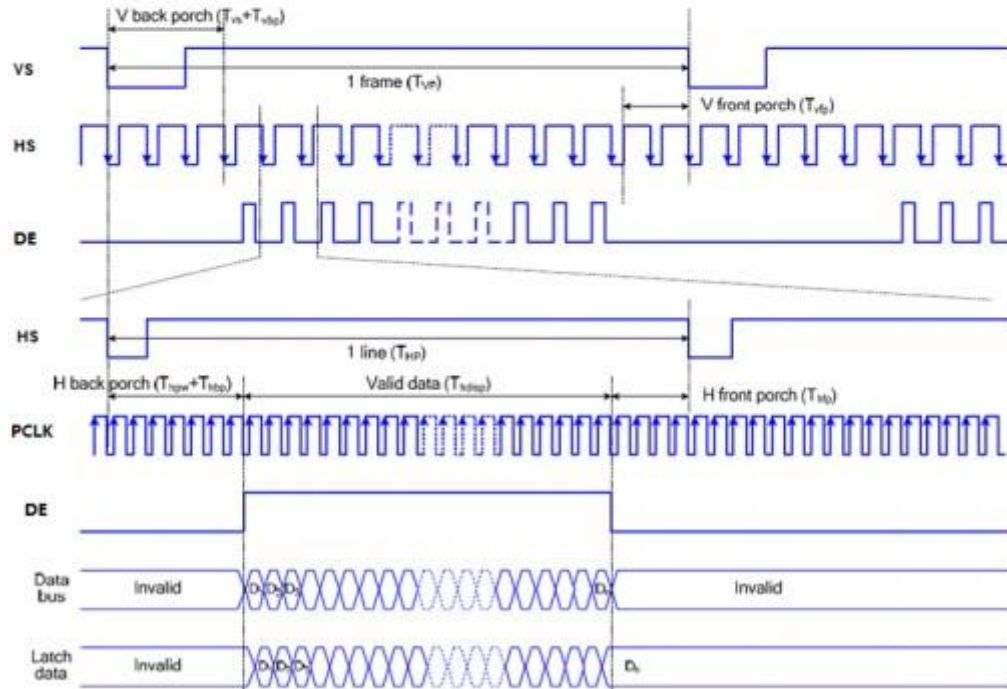
### 6.1.2 RGB Interface Mode Selection

NV3052CGRB supports two kinds of RGB interface, DE mode and SYNC mode. The table shown below uses command 23h to select RGB interface mode.

sync_mode[1:0]	RGB Mode
00	SYNC+DE mode
01	SYNC mode
10	DE mode
11	SYNC+DE mode

### 6.1.3 RGB Interface Timing

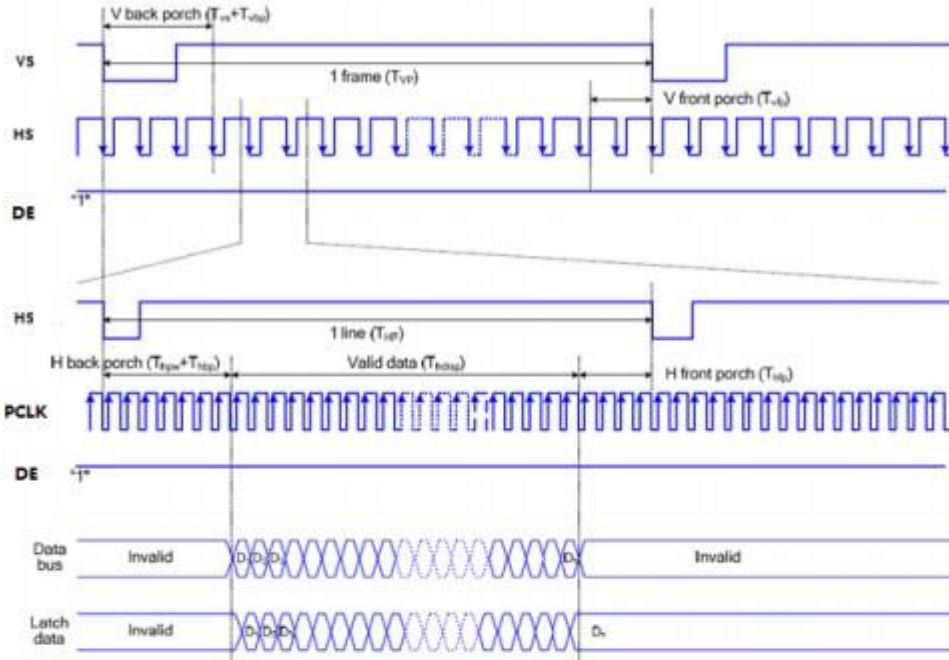
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in host must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.



Timing chart of RGB interface SYNC mode

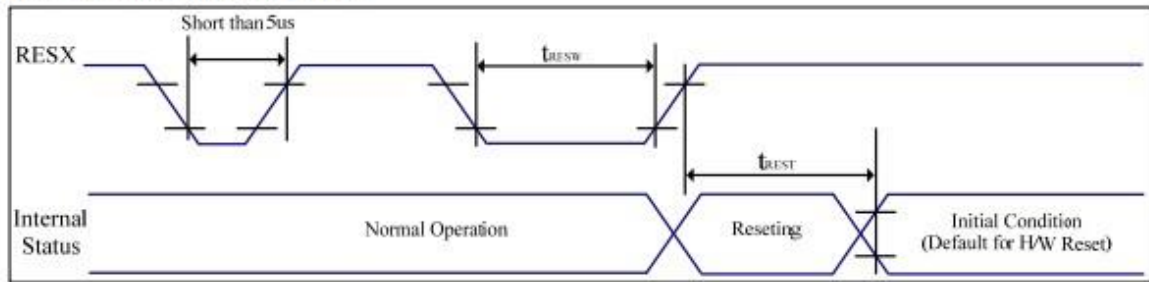
Below Table provide the timing parameter by external Vertical-cycle  
(Resolution for 720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	hpw	-	2	-	PCLK
Horizontal Back Porch	hbp	-	42	-	PCLK
Horizontal Front Porch	hfp	-	44	-	PCLK
Hsync+ HBP+ HFP	-	-	88*Note1	-	PCLK
Horizontal Address (Display area)	hdisp	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	VS	-	2	-	Line
Vertical Back Porch	vbp	-	14	-	Line
Vertical Front Porch	vfp	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	vdisp	-	1280	-	Line
Vertical cycle	-	-	16.66	16.181	ms
Frame-Rate	-	-	60	61.8	Hz

"-" means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

### Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
$T_{resw}$	*1) Reset low pulse width	RESX	10	-	-	-	us
$T_{rest}$	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

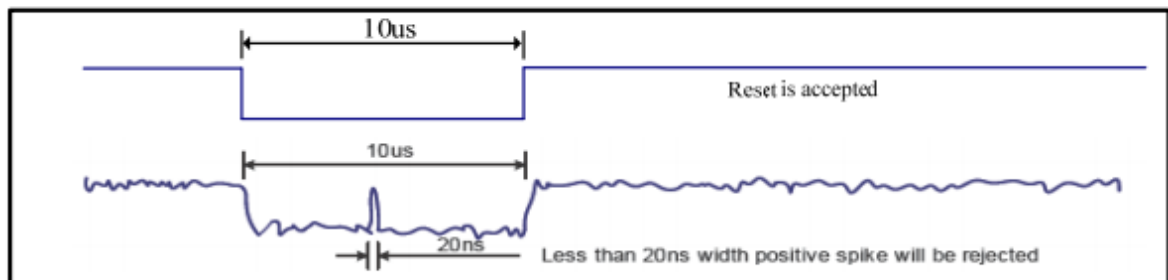
Note 1: Due to an electrostatic discharge on RESX line, spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode), then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time ( $T_{rest}$ ) which lasted 5ms. The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.



## 6. Optical Characteristics

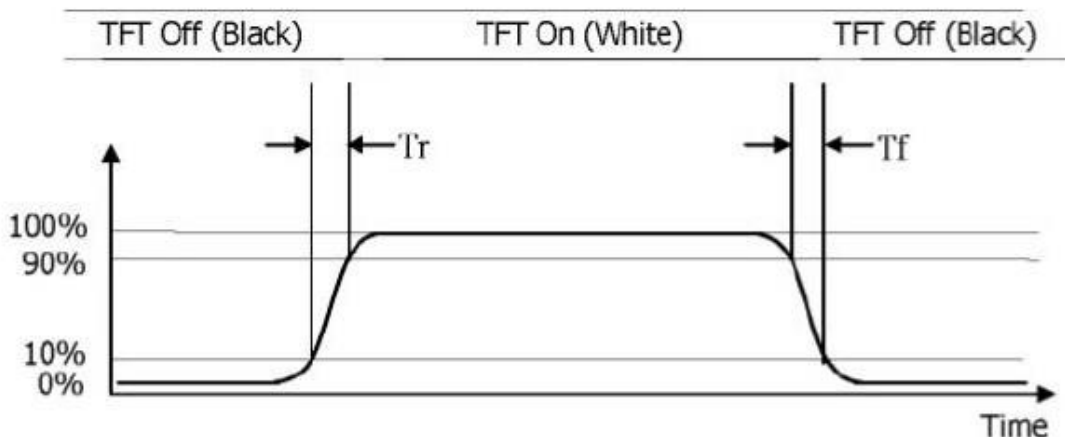
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark		
Viewing Angle range	Horizontal	$\Theta_3$	CR > 10	80	85	-	Deg.	Note 1		
		$\Theta_9$		80	85	-	Deg.			
	Vertical	$\Theta_{12}$		80	85	-	Deg.			
		$\Theta_6$		80	85	-	Deg.			
Luminance Contrast ratio		CR		1000	1200	-		Note 2		
Transmittance (pol)		T(%)		4.55	5.35	-	%	@Silicate BLU POL:HC+ Clear Note 3		
White luminance uniformity		$\Delta Y$					%			
White Chromaticity		$x_w$	$\Theta = 0^\circ$ (Center) Normal Viewing Angle	0.262	0.292	0.322		CF @C Light Note 4		
		$y_w$		0.307	0.337	0.367				
Reproduction of color	Red	$x_R$		0.620	0.650	0.680				
		$y_R$		0.292	0.322	0.352				
	Green	$x_G$		0.250	0.280	0.310				
		$y_G$		0.533	0.563	0.593				
	Blue	$x_B$		0.105	0.135	0.165				
		$y_B$		0.111	0.141	0.171				
Response Time (Rising + Falling)		$T_{RT}$		Ta= 25° C $\Theta = 0^\circ$	-	30	35		ms	Note 5

**Note :**

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of  $\theta = 0^\circ$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer(HC+Clear) & silicate BLU (Film structure is on Table 4.1)
4. The color chromaticity coordinates specified in the above Table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as **FIGURE 1** shown in Appendix. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_f$ .

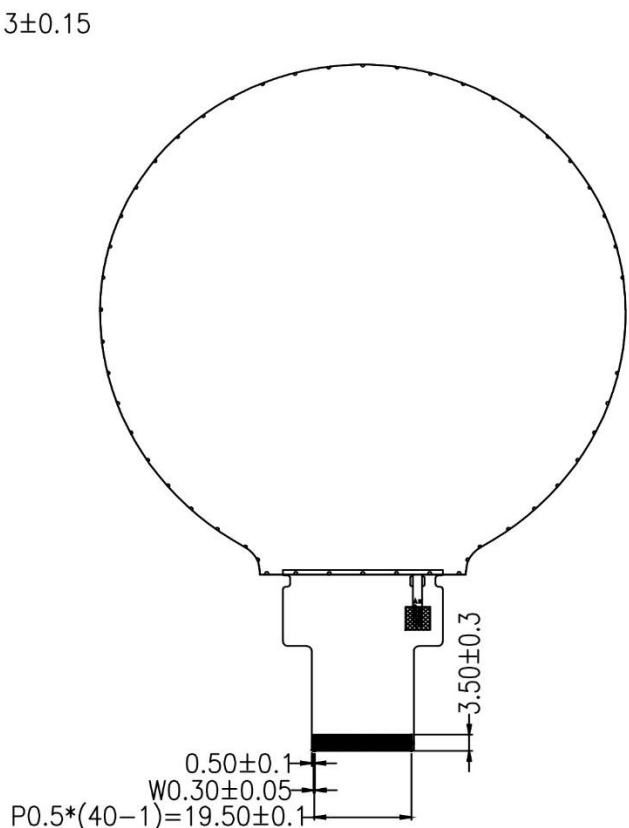
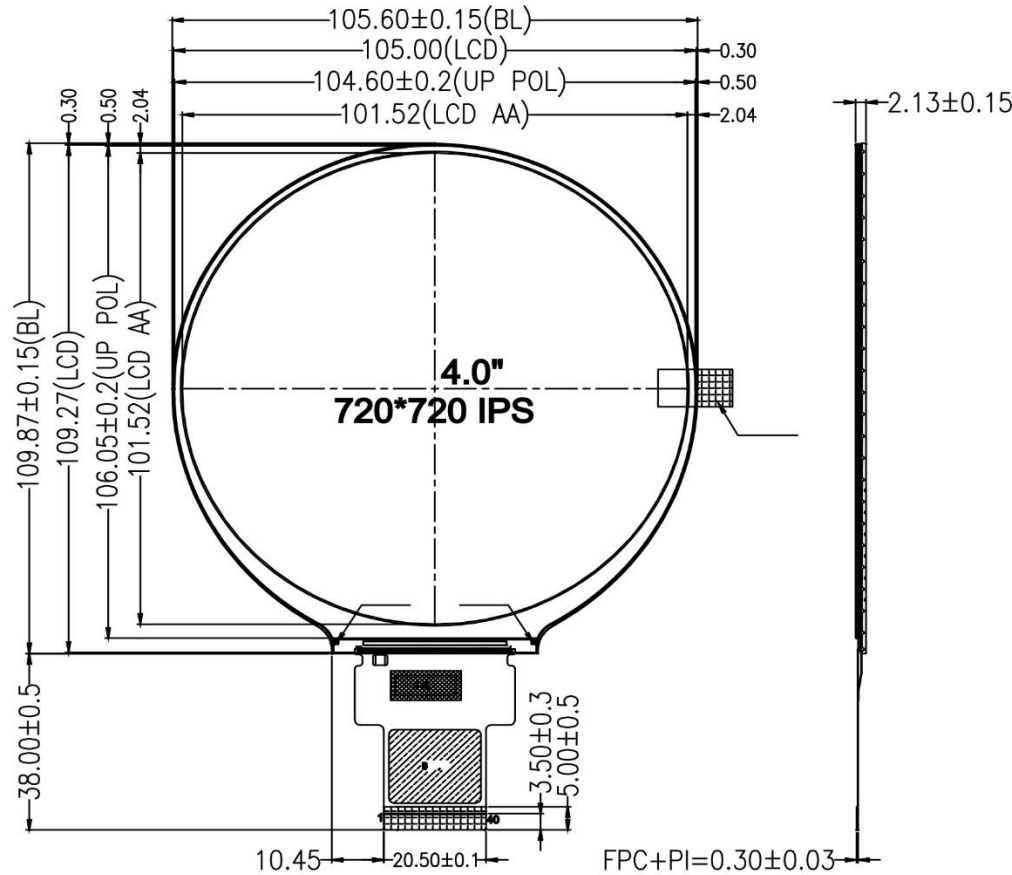


**Figure1 Response Time Testing**

## 7. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+70°C / 96H	1. Functional test is OK. Missing Segment, short, unclear segment non-display, display abnormally and liquid crystal leakage. un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+60°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature / Humidity storage	50°C x 90%RH / 96H	
6	Thermal and cold shock	Static state, -20°C (30min) ~60°C (30min), 50 cycles	

# 8. Dimensions



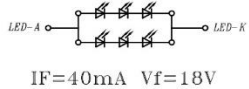
N0	SYMBOL
01	LEDA
02	LEDK
03	VCC(3.3V)
04	GND
05	GND
06	DEN
07	VSYNC
08	HSYNC
09	CLK
10	B7
11	B6
12	B5
13	B4
14	B3
15	B2
16	B1
17	B0
18	G7
19	G6
20	G5
21	G4
22	G3
23	G2
24	G1
25	G0
26	R7
27	R6
28	R5
29	R4
30	R3
31	R2
32	R1
33	R0
34	RESET
35	CS
36	SCL
37	SDA
38	GND
39	VCC(3.3V)
40	GND

**NOTES:**

1. DISPLAY TYPE: 4.0", 720\*720 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC: NV3052CGRB
5. LCM (White 9 AVG 1/9) :  
Brightness: 600cd/m<sup>2</sup>(TYP)  
Uniformity: 80%(MIN)
6. BACK LIGHT: 6 chip white LEDs If=40mA, Vf=16.8V-19.2V
7. OPERATING TEMP: -20° C TO 70° C, STORAGE TEMP: -30° C TO 80° C
8. \* Critical Parameter, ( ) ref Parameter, [ ] cpk Parameter  
Unspecified Tolerances: ±0.20mm  
Modification mark:
9. SUGGESTION: TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

FPC+PI=0.30±0.03

**LED CIRCUIT DIAGRAM:**



**HIGHNESS MICROELECTRONICS PVT. LTD.**  
 One of a kind

Part No. : HM040HD111TV		
DRAWING BY AKASH SHINDE	DIMENSION UNIT MM	ISSUE DATE 12 / 10 / 2023
CHECKED BY RAJESH PATIL	SCALE NOT TO SCALE	REV -